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SEARCH REQUEST FORM

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****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

_____

Earliest Priority Filing Date: _____

For Sequence Searches Only *Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

_____

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STAFF USE ONLY	Type of Search	Vendors and cost where applicable
Searcher: _____	NA Sequence (#)_____	STN _____
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Date Completed: _____	Litigation _____	Lexis/Nexis _____
Searcher Prep & Review Time: _____	Fulltext _____	Sequence Systems _____
Clerical Prep Time: _____	Patent Family _____	WWW/Internet _____
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Search Results -

Terms	Documents
(l1 or l2) and ((l5 and l6) or (l7 and l8))	6

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Nothing found here

Refine Search: (l1 or l2) and ((l5 and l6) or (l7 and l8)) Clear

Search History

Today's Date: 7/3/2001

DB Name	Query	Hit Count	Set Name
TDBD	(l1 or l2) and ((l5 and l6) or (l7 and l8))	6	L10
TDBD	(l1 or l2 or l3) and ((l5 and l6) or (l7 and l8))	60	L9
TDBD	dualport$ or (dual or two or 2 or multiple or multi or dual or separate or different or twin or second$ or double) near5 port$ or multiport$	1850	L8
TDBD	singleport$ or (single or one or 1) near5 port$	1525	L7
TDBD	writ$ near5 port$	295	L6
TDBD	read$ near5 port$	389	L5
TDBD	ram$ or memor$	12208	L4
TDBD	logic$ adj2 (unit$ or device$ or circuit$$ or microcircuit$ or chip$ or module$ or board$ or block$ or microchip$ or ic or apparatus)	3320	L3
TDBD	spld$ or cpld$ or fpga$ or fpic$ or field adj programmable adj (gate$ or interconnect$ or inter adj connect$)	21	L2
TDBD	(programmable adj2 logic$)	282	L1

19/5/21 (Item 8 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00565674 **Image available**

FPGA ARCHITECTURE HAVING RAM BLOCKS WITH PROGRAMMABLE WORD LENGTH AND WIDTH AND DEDICATED ADDRESS AND DATA LINES

ARCHITECTURE FPGA A BLOCS DE MEMOIRE RAM POUR LONGUEUR ET LARGEUR DE MOT PROGRAMMABLES ET POUR LIGNES D'ADRESSES ET DE DONNEES SPECIALISEES

Patent Applicant/Assignee:
XILINX INC, XILINX, INC. , 2100 Logic Drive, San Jose, CA 95124 , US
Inventor(s):
YOUNG Steven P, YOUNG, Steven, P. , 6131 Paso Los Cerritos, San Jose, CA 95120 , US

Patent and Priority Information (Country, Number, Date):
Patent: WO 9810517 A1 19980312
Application: WO 97US10279 19970616 (PCT/WO US9710279)
Priority Application: US 96708247 19960903
Designated States: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **H03K-019/177** ;
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 11795

English Abstract
A structure in which blocks of random access memory, or RAM, are integrated with FPGA configurable logic blocks. Routing lines which access configurable logic blocks also access address, data, and control lines in the RAM blocks. Thus, the logic blocks of the FPGA can use these routing lines to access portions of RAM. In one embodiment, dedicated address and data lines access the RAM blocks of the present invention and are connectable to routing lines in the interconnect structure. These lines allow RAM blocks and arrays of RAM blocks to be configured long, wide, or in between, and allow logic blocks to conveniently access RAM blocks in a remote part of the chip. Access to the RAM blocks is efficient in any RAM configuration. Bidirectional buffers or pass devices segment the address and data lines at each RAM block so that a selectable number of RAM blocks can operate together as a RAM. In another embodiment, dedicated data lines are programmably connectable in a staggered arrangement so that RAM blocks can be connected over a long distance without conflict between the RAM blocks.

19/3,K/21 (Item 8 from file: 349)
DIALOG(R)File 349:PCT Fulltext

00565674 **Image available**

FPGA ARCHITECTURE HAVING RAM BLOCKS WITH PROGRAMMABLE WORD LENGTH AND WIDTH AND DEDICATED ADDRESS AND DATA LINES

ARCHITECTURE FPGA A BLOCS DE MEMOIRE RAM POUR LONGUEUR ET LARGEUR DE MOT PROGRAMMABLES ET POUR LIGNES D'ADRESSES ET DE DONNEES SPECIALISEES

Patent Applicant/Assignee:
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YOUNG Steven P, YOUNG, Steven, P. , 6131 Paso Los Cerritos, San Jose, CA 95120 , US

Patent and Priority Information (Country, Number, Date):
Patent: WO 9810517 A1 19980312
Application: WO 97US10279 19970616 (PCT/WO US9710279)
Priority Application: US 96708247 19960903
Designated States: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Filing Language: English
Fulltext Word Count: 11795

Main International Patent Class: **H03K-019/177** ;
Fulltext Availability:
Detailed Description

Detailed Description

... Default Input" which was filed 07-26-95 by Steven P. Young and issued 05-14-96.

FIELD OF THE INVENTION

The invention relates to **programmable logic** devices formed. in integrated circuits and more particularly to field **programmable logic** devices or field programmable gate arrays.

BACKGROUND OF THE INVENTI

A field programmable gate array (FPGA) comprises an array of **programmable logic** blocks which can be programmably interconnected to each other to provide a logic function desired by a user. U. S. Patent 4,870,302, reissued...

...by Concurrent Logic, Inc. describe other FPGA architectures.

These patents and application are also incorporated herein by reference. The Xilinx 1994 Data Book entitled "The **Programmable Logic** Data Book", available from Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124 describes several FPGA products. As illustrated in the Xilinx data book, for...

...array of configurable logic blocks. The programmable routing matrix includes means for connecting logic blocks to each other. Thus an FPGA provides a combination of **programmable logic** and programmable connections to a general routing structure.

In a typical FPGA application, the PIPs are turned on ahead of time by loading appropriate values...dual port RAM 131. A dual port RAM provides two independent sets of address, data, and control lines for accessing the same memory locations.

A **dual port RAM** is useful when a user wants to read or write to two addresses in the same **memory** at the same time. For example, a FIFO which receives bursts of data from an external source and stores the data for internal processing makes good use of the **dual ports** , using **one port** for being written to from the external source and the other for being read by internal logic.

In Fig. 2, as in Fig. 1B, extending...the regions of the respective RAM blocks.

Dual port RAM Configurations

Since each 256x9 RAM is a dual port RAM, it can be configured as **two** separate **single -port** 128x9 RAMs, or as **one single -port** 128x18 **RAM** . Recall that all 256 x 9 = 2304 **RAM** bits are addressable from both address buses.

To form two 128x9 RAMs, one of the eight address bits, for example the most significant address bit, is permanently set to one state on the address bus for **one port** and the other state for the other port. This causes half the **RAM** to be addressed by the seven remaining bits on one address bus and half by the seven bits on the other address bus. The least significant seven address lines of **one** address **port** are connected to **one** set of seven vertical address lines and the least significant seven is address lines of the other address port are connected to another set of seven vertical address lines. The data-in **ports** are connected to **separate** data-in lines and the data-out **ports** are connected to **separate** data-out lines.

To form **one single -port** 128x18 **RAM** , the most significant bit in **one** address **port** is connected to the enabling voltage source, for example logical 1 and the most significant bit in the other address port is connected to ground. The remaining seven address lines from the **two ports** are connected to the same seven vertical address lines. Thus any address on the seven vertical address lines addresses two sets of **RAM** cells.

The eighteen vertical data-out lines are connected to the eighteen data-out lines of the two ports and thus receive the contents of... patterns of PIPs allow other options. As discussed above, a more dense pipulation gives more options but requires more chip area to implement.

```
File 275:Gale Group Computer DB(TM) 1983-2001/Jun 29
         (c) 2001 The Gale Group
File 583:Gale Group Globalbase(TM) 1986-2001/Jul 02
         (c) 2001 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2001/Jul 02
         (c) 2001 The Gale group
File 621:Gale Group New Prod.Annou.(R) 1985-2001/Jul 02
         (c) 2001 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2001/Jul 02
         (c) 2001 The Gale Group
File  16:Gale Group PROMT(R) 1990-2001/Jul 02
         (c) 2001 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2001/Jul 02
         (c)2001 The Gale Group
File 623:Business Week 1985-2001/Jul W1
         (c) 2001 The McGraw-Hill Companies Inc
File 624:McGraw-Hill Publications 1985-2001/Jul 03
         (c) 2001 McGraw-Hill Co. Inc
File  98:General Sci Abs/Full-Text 1984-2001/May
         (c) 2001 The HW Wilson Co.
File 553:Wilson Bus. Abs. FullText 1982-2001/May
         (c) 2001 The HW Wilson Co
File  88:Gale Group Business A.R.T.S. 1976-2001/Jul 03
         (c) 2001 The Gale Group
File  15:ABI/Inform(R) 1971-2001/Jul 03
         (c) 2001 ProQuest Info&Learning
File 635:Business Dateline(R) 1985-2001/Jul 03
         (c) 2001 ProQuest Info&Learning
File   9:Business & Industry(R) Jul/1994-2001/Jul 02
         (c) 2001 Resp. DB Svcs.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2001/Jul W1
         (c) 2001 CMP
File 674:Computer News Fulltext 1989-2001/Jun W4
         (c) 2001 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2001/Jul 02
         (c) 2001 The Dialog Corp.
File 369:New Scientist 1994-2001/Jun W2
         (c) 2001 Reed Business Information Ltd.
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2001/Jul 03
         (c) 2001 PR Newswire Association Inc
File 634:San Jose Mercury  Jun 1985-2001/Jun 30
         (c) 2001 San Jose Mercury News
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS

Set     Items   Description
S1      38230   PROGRAMMABLE(2W)LOGIC?
S2      30236   SPLD? ? OR CPLD? ? OR FPGA? ? OR FPIC? ? OR FIELD()PROGRAM-
             MABLE()(GATE? ? OR INTERCONNECT? ? OR INTER()CONNECT? ?)
S3      69693   LOGIC?(2W)(UNIT? ? OR DEVICE? ? OR CIRCUIT?? OR MICROCIRCU-
             IT? ? OR CHIP? ? OR MODULE? ? OR BOARD? ? OR BLOCK? ? OR MICR-
             OCHIP? ? OR IC OR APPARATUS)
S4    1673404   RAM? ? OR MEMOR???
S5       4638   READ???(3N)PORT? ?
S6       2339   WRIT???(3N)PORT? ?
S7      86420   SINGLEPORT? ? OR (SINGLE OR ONE OR 1)(3N)PORT? ?
S8     130887   DUALPORT? ? OR (DUAL OR TWO OR 2 OR MULTIPLE OR MULTI OR D-
             UAL OR SEPARATE OR DIFFERENT OR TWIN OR SECOND? OR DOUBLE)(3N-
             )PORT? ? OR MULTIPORT? ?
S9        557   S5(10N)S6
```

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S10      22345   S7(10N)S8
S11         50   S1(50W)S9:S10
S12         30   RD (unique items)
S13        228   S5(10N)S6(10N)S4
S14       4179   S7(10N)S8(10N)S4
S15         45   S2(25W)S13:S14
S16         24   RD (unique items)
S17         20   S16 NOT S12
S18         65   S3(25W)S13:S14
S19         40   RD (unique items)
S20         23   S19 NOT (S12 OR S17)
```

12/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02327774 SUPPLIER NUMBER: 55660024 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Atmel Announces Embedded FPGA Cores for Enable Programmable ASICS; Programmable ASICs, ASSPs. (AT40K field-programmable gate arrays) (Product Announcement)
EDGE: Work-Group Computing Report, NA
Sept 6, 1999
DOCUMENT TYPE: Product Announcement LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 609 LINE COUNT: 00054

... has developed a supporting design tool suite. This is not a technology announcement," Rosenberg continued. "It is a product announcement. Designers who want to embed **programmable logic** in an ASIC can do it today, and have design tools to support their products."
Atmel's AT40K is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, **dual port / single port** SRAM, 8 global clocks, Cache Logic partial or full reconfigurability, on-the-fly, and automatic component generators. With its 8-sided logic cell and orthogonal...

12/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02229821 SUPPLIER NUMBER: 53098251 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Financial: Cypress Reports Profitable Q398 Revenue $126 Million, 1-Cent EPS. (Company Financial Information)
EDGE: Work-Group Computing Report, NA
Oct 19, 1998
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 680 LINE COUNT: 00103

TEXT:
...new products also contributed in the quarter. The company realized revenue on nine new products including: o The Ultra37000(TM) CPLDs, a new family of **programmable logic** devices with industry-leading performance, flexibility for designers to make logic changes without timing or pin-assignment changes, and high density up to 512 macrocells. o A **1** -Mbit **dual -port** SRAM that offers industry-leading performance at 100 MHz, the largest density of any dual-port on the market. o A family of 12 high...

12/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02117718 SUPPLIER NUMBER: 19912663 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Reformed GateField focuses on PLDs. (the GF260F field-programmable gate arrays) (Product Announcement)
Brown, Peter
Electronic News (1991), v43, n2190, p14(1)
Oct 20, 1997
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 526 LINE COUNT: 00044

...ABSTRACT: from 43,000 to 123,000 gates. The company, known formerly as Zycad, has divested its EDA and non-profitable businesses and will focus on **programmable logic** . The GF260F uses GateField's ProASIC technology and is the most flexible, non-volatile reprogrammable FPGA from the company. The products are designed for **single -port** or **dual -port** SRAM and

FIFO operation, synchronous or asynchronous operation, and multiple memories. They will be used in networking, telecommunications, multimedia and data processing applications as well...

12/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2001 The Gale Group. All rts. reserv.

01955839 SUPPLIER NUMBER: 18221425 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Literature watch.
Microprocessor Report, v10, n5, p16(1)
April 15, 1996
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 812 LINE COUNT: 00067

... combines a 32-bit CPU and 16 Mbits of DRAM on a single chip. Dave Bursky, Electronic Design, 3/4/96, p. 67, 4 pp.

Programmable Logic

CPLDs add dedicated memory, counters to up performance. Lattice Semiconductor can combine a FIFO, or **dual** - or **single -port** RAM, with its CPLDs. Dave Bursky, Electronic Design, 3/4/96, p.141, 2 pp.

Reconfigurable logic: hardware speed with software flexibility. Reconfigurable logic lets...

12/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2001 The Gale Group. All rts. reserv.

01913180 SUPPLIER NUMBER: 18096009 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Lattice adds memory modules to PLD family. (Lattice Semiconductor's ispLSI/PLSI 6192XX in-system complex programmable logic devices)(Product Announcement)
Electronic News (1991), v42, n2107, p52(1)
March 11, 1996
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 675 LINE COUNT: 00057

ABSTRACT: Lattice Semiconductor recently introduced its ispLSI/PLSI 6192XX line of in-system programmable (ISP) complex **programmable logic** devices (CPLDs). The ispLSI 6192FF features two-port FIFO memory, the ispLSI 6192DM includes **dual -port** RAM and the ispLSI 6192SM includes **single -port** RAM. The devices integrate register/counter modules and dedicated memory with general-purpose programmable logic in a 25,000-gate device. Lattice is attempting to...

12/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2001 The Gale Group. All rts. reserv.

01250833 SUPPLIER NUMBER: 06790453 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Boost DRAM performance with SRAM caching scheme. (dynamic and static random access memory schemes for 80386-based microcomputers)
Langston, Jim
Electronic Design, v36, n13, p107(6)
June 9, 1988
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 3396 LINE COUNT: 00246

... signal is connected to the inputs as required. At 20 MHz, there are 10 ns for decoding. Decoding is most commonly accomplished with a fast **programmable logic** device, such as the 16L8, with up to 8 minterms.

One type of main memory taht shouldn't be cached is the **dual -port**

memory. The 385 snoop bus can only monitor **one port** . Consequently, the other port might fill the main memory without the cache knowing it, and the cache would have incorrect data. Optionally, ROM can also...

12/3,K/7 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2001 The Gale Group. All rts. reserv.

02849273 Supplier Number: 72691731 (USE FORMAT 7 FOR FULLTEXT)
Cypress Samples World's First 2.5 Gbps Programmable PHY.
Business Wire, p0530
April 3, 2001
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 863

... and insert their own custom logic."
"Cypress is first to market with the PSI2G100, ahead of both pure-play data communications/physical-layer companies and **programmable - logic** specialists," said Ralph Schmitt, Cypress vice president of sales and marketing. "Those companies will need to find partners or make acquisitions to achieve the same level of integration and customization that Cypress can deliver today."
The PSI2G100 has abundant communications memory, 48 Kbits of **Dual Port** /FIFO and 192 Kbits of **single -port** RAM for memory-intensive networking functions like queuing, head-of-line blocking and distributed switching. InfiniBand compliant, the PSI2G100 is a key component in Cypress ...

12/3,K/8 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2001 The Gale Group. All rts. reserv.

01825287 Supplier Number: 54073110 (USE FORMAT 7 FOR FULLTEXT)
Lucent Technologies Broadens FPGA Offering; OEMs LeonardoSpectrum Synthesis Solution from Exemplar Logic.
Business Wire, p0076
March 11, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 476

... said Barry Britton, FPGA marketing director for Lucent Microelectronics. "FPSCs combine an embedded system solution, such as PCI, with up to 60 K gates of **programmable logic** . LeonardoSpectrum's ability to support our IP timing and loading models, automatically infer **single -** and **dual -port** RAMs and efficiently map users' HDL code to our new soft-wired LUTs makes it a logical choice for our customers."
A Comprehensive Synthesis Environment...

12/3,K/9 (Item 3 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2001 The Gale Group. All rts. reserv.

01727393 Supplier Number: 53078496 (USE FORMAT 7 FOR FULLTEXT)
Cypress Reports Profitable Q398 Revenue $126 Million, 1-Cent EPS.
Business Wire, p1130
Oct 13, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1143

... new products also contributed in the quarter. The company realized

revenue on nine new products including: -0-

-- The Ultra37000(TM) CPLDs, a new family of **programmable logic** devices with industry-leading performance, flexibility for designers to make logic changes without timing or pin-assignment changes, and high density up to 512 macrocells.

-- A **1** -Mbit **dual -port** SRAM that offers industry-leading performance at 100 MHz, the largest density of any dual-port on the market.

-- A family of 12 high-speed...

12/3,K/10 (Item 4 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01726118 Supplier Number: 53074215 (USE FORMAT 7 FOR FULLTEXT)
Altera Ships First Enhanced, 0.25-Micron FLEX(R) 10KE Device.
PR Newswire, p9251
Oct 12, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 950

Dual-**Port** RAM With Independent **Read /Write Ports**
* 0.25-Micron, Five-Layer Metal CMOS SRAM Process
* Pin-Compatible With FLEX(R) 10K and 10KA Devices
SAN JOSE, Calif., Oct. 12 /PRNewswire/ -- Altera Corporation (Nasdaq: ALTR) today announced the availability of the EPF10K50E **programmable logic** device, the first 0.25-micron, 2.5-V version of the FLEX(R) 10K architecture that features enhanced dual-port RAM and ultra-high...

...10K customer base another performance boost of more than 30 percent over our industry leading FLEX 10KA devices. In addition, FLEX 10KE's embedded dual-**port** RAM enables simultaneous **read /write** operations to independent **ports** for more efficient utilization of RAM-bits per silicon area, allowing more room for the integration of megafunctions such as a Reed Solomon Encoder/Decoder...

12/3,K/11 (Item 5 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01167641 Supplier Number: 42204460 (USE FORMAT 7 FOR FULLTEXT)
80486SX PC/AT COMPUTER BRINGS AFFORDABLE HIGH PERFORMANCE TO VMEbus APPLICATIONS
News Release, pN/A
July 8, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 261

... or 16 Mbytes of dual-access DRAM, ROM-resident BIOS with diagnostics, 8 Kbytes of VME cache memory, battery-backed time-of-day clock, software-**programmable** byte swapping **logic , two** serial **ports , one** parallel **port** and a watchdog timer.

The XVME-697 is a complete 32-bit VMEbus master/slave which allows easy access to VMEbus Short I/O, Standard...

12/3,K/12 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03990350 Supplier Number: 53094642 (USE FORMAT 7 FOR FULLTEXT)
-CYPRESS: Cypress reports profitable Q3 98 -- Revenue $126 million, 1-cent EPS.
M2 Presswire, pNA
Oct 16, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 615

... emphasis on new products also contributed in the quarter. The company realised revenue on nine new products including:
-- The Ultra37000 CPLDs, a new family of **programmable logic** devices with industry-leading performance, flexibility for designers to make logic changes without timing or pin-assignment changes, and high density up to 512 macrocells.
-- A **1** -Mbit **dual -port** SRAM that offers industry-leading performance at 100 MHZ, the largest density of any dual-port on the market.
-- A family of 12 high-speed...

12/3,K/13 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

08707615 Supplier Number: 75433498 (USE FORMAT 7 FOR FULLTEXT)
Pulling The PLD Market Out Of The Doldrums -- No one knows exactly when the recovery will begin, but PLD executives expect new technologies and applications, particularly in communications, to spur growth. (Industry Trend or Event)
Mayer, John H.
EBN, p51
June 11, 2001
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3104

... in a family of Programmable Serial Interface (PSI) chips. The PSI2G100 combines one to eight 2.5Gbit/s serdes links with 100,000 gates of **programmable logic** for control functions. The device also adds 48Kbits of **dual -port** memory and 192Kbits of **single -port** RAM to support queuing and distributed switching. The primary target for this new device is InfiniBand and similar backplane networking applications.
"It's precision-

12/3,K/14 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06495820 Supplier Number: 55191830 (USE FORMAT 7 FOR FULLTEXT)
Embedded Logic And Memory Find A Home In FPGAs.
Bursky, Dave
Electronic Design, v47, n14, p43
July 12, 1999
Language: English Record Type: Fulltext Abstract
Document Type: Magazine/Journal; Trade
Word Count: 4178

... logic and a string of 256-word-by-9-bit embedded memory blocks (14 to 138 kbits). These blocks, in turn, can be configured as **single** - or **dual -port** RAMs or as a FIFO buffer (Fig. 3).
Based on 0.25-[micro]m design rules and four levels of metal

interconnect, the fine-grain...

...DMA controllers and a total of six FIFO buffers to ease data-transfer issues (Fig. 5). The QL5064 packs about 45 kgates of high-speed **programmable logic** , too.

In addition to the PCI core with dedicated FIFO memories, the QL5064 includes 12 kbits of RAM (consisting of eight 1152-bit blocks) that can each be configured as **single** or **dual -port** memory, or as a FIFO buffer. The other chips in the Quick-PCI family include a 32-bit Slave-only core, a 32-bit Master...

12/3,K/15 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

12937234 SUPPLIER NUMBER: 68534452 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Hot 100 Products 2000 (1).(Technology Information)
EDN, 45, 25, 59
Dec 7, 2000
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3029 LINE COUNT: 00248

... 514 at www. rscahners.ims.ca/ednmag/

FPGA HEAVYWEIGHT GETS SERIOUS ABOUT HYBRIDS. Altera this summer announced its Excalibur program, initially targeting the Apex 20K **programmable -logic** family and consisting of the Nios processor soft core and both ARM (www.arm.com) and MIPS (www.mips.com) hard cores. Altera's XA10 integrates a 200-MHz ARM922 core, including 8 kbytes each of instruction and data cache; 256 kbytes of **dual -port** SRAM; and 128 kbytes of **single -port** SRAM. The device will be available for sampling by year-end and will enter volume production in the first quarter of 2001. Altera plans to...

12/3,K/16 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

12905177 SUPPLIER NUMBER: 68146157 (USE FORMAT 7 OR 9 FOR FULL TEXT)
FPGA heavyweights get serious about hybrids.(Company Business and Marketing)
Dipert, Brian
EDN, 45, 24, 30
Nov 23, 2000
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 637 LINE COUNT: 00071

... SRAM; and a single-cycle, 32 x 16-bit multiply-accumulator. Both ARM- and MIPS-based architectures will also come in smaller variants with less **single** - and **dual -port** RAM and **programmable logic** by midyear 2001, according to the company. And Altera has resurrected its MPLD (mask-**programmable logic** -device) program to provide lower cost, high-volume production variants of most of the devices. Table 1 shows planned ARM device features, and Table 2...

...Logic-array blocks (programmable)	416	1664
Embedded system blocks (programmable)	26	104
Maximum RAM (programmable)	53,248	212,992
Maximum I/O pins	178	360
Single -port SRAM	32 kbytes	128 kbytes
Dual -port SRAM	16 kbytes	64 kbytes

ARM-based device features	EPXA3
Maximum system gates (programmable)	1,772,000

Typical gates (**programmable**)(*)	1 million
Logic elements (**programmable**)	38,400
Logic -array blocks (programmable)	3840
Embedded system blocks (programmable)	160
Maximum RAM (programmable)	327,680
Maximum I/O pins	521
Single -port SRAM	256 kbytes
Dual -port SRAM	128 kbytes

TABLE 2--ALTERA'S END-OF-2001 DEVICE PRICES

	XA1	XA4	XA10
Price	XM1	XM4	XM10
100 units	$100	$500	$2000
10...			

12/3,K/17 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

12559290 SUPPLIER NUMBER: 65091406 (USE FORMAT 7 OR 9 FOR FULL TEXT)
EDN's first annual Programmable-logic directory.(Buyers Guide)
Dipert, Brian
EDN, 45, 17, 54
August 17, 2000
DOCUMENT TYPE: Buyers Guide ISSN: 0012-7515 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 8435 LINE COUNT: 00712

... s marketing might indicate are possible.
Apex 20KE, the latest iteration of the product family, enables you to use the EABs not only for implementing **single** - and **dual -port** RAM and FIFOs, but also for very small CAMs. The recently introduced Acex 1K family is basically Flex 10KE built on a smaller lithography process...

...provider of both FPGAs and ASICs. The company not only produces FPGA-plus-ASIC chips of its own but also supplies you with embedded programmable-**logic** cores for your ASIC-based designs. Atmel is also a nonvolatile-memory manufacturer; the company sells EEPROM-based (therefore in-system-programmable and -reprogrammable) configuration memories for its FPGAs, as well as for those of other **programmable -logic** vendors.
AT A GLANCE
* Second-generation FPGAs from Atmel have multiplication in mind.
* An 8-bit AVR controller makes system on chip a reality.
* Embedded cores bring **programmable logic** to your ASICs.
LUCENT TECHNOLOGIES
Lucent Technologies originally entered the FPGA business as an alternative supplier of Xilinx's XC3000 FPGAs, which Lucent referred to as its ATT3000 series. From those humble beginnings, the company has made significant progress in establishing its own identity as a **programmable -logic** vendor and taking advantage of its internal FPGA and ASIC capabilities. Given the parent company's telecommunications heritage and the high percentage of FPGAs sold...

...four registers into each PFU (programmable function unit). Like Xilinx, and unlike Altera, each LUT grouping can alternatively find use as a synchronous or asynchronous, **single** - or **dual -port** , RAM or ROM block. Each PFU also contains eight tristate buffers

12/3,K/18 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

11589883 SUPPLIER NUMBER: 55897009 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Core-Based Design Leads The Way To Flexible System Solutions.
BURSKY, DAVE
Electronic Design, 45, 9, 38
May 1, 1997
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2968 LINE COUNT: 00240

... includes lookup table combinatorial logic, an abundant number of flip-flops, and PAL-type decoder blocks, all grouped in a twin-nibble fashion. The basic **programmable logic** cell contains a programmable function unit (PFU) and a supplemental logic and interconnection cell (SLIC). Together, they provide a flexible building block that supports typical glue logic and most common functions that make up behavioral-level code, such as adders, subtractors, counters, accumulators, comparators, multipliers, and **single** -and **dual** -**port** RAMs.

A research project at the Department of Electrical and Computer Engineering at the University of Toronto, Ontario, Canada, has led to the development of...

12/3,K/19 (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

10683467 SUPPLIER NUMBER: 53365124 (USE FORMAT 7 OR 9 FOR FULL TEXT)
SRAMs strive to specialize.(static random access memory; includes contact information of manufacturers)
Dipert, Brian
EDN, 62(1)
Nov 5, 1998
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 6842 LINE COUNT: 00567

... with different widths. However, multiport SRAMs offer more functions than their FIFO counterparts.

(Figure A ILLUSTRATION OMITTED)

Unlike unidirectional FIFO buffers, multiport SRAMs let you **read** and write both **ports** . They also enable full random access of any location in the memory array, whereas both FIFO and last-in-first-out (LIFO) access protocols imply...

...and less than comparison results. Binary CAMs integrate the external logic that yet another CAM alternative (employing a standard SRAM and separate microcontroller, ASIC, or **programmable** -**logic** device) uses.

Hashing provides no consistent, deterministic search delay. (Some searches complete faster than others.) However, you can still calculate the maximum delay latency, which may be sufficient for your application. Motorola's NetRAMs externally appear to work just like standard synchronous **dual** -**port** SRAMs; however, NetRAMs internally **read** and **write** **one** **port** on **one** edge of the input clock and the other port on the opposite edge. You should consider NetRAMs if both of your system buses operate from ...

12/3,K/20 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

10272530 SUPPLIER NUMBER: 20543402 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Budding FPGAs beat last year's crop. (field programmable gate array)
Dipert, Brian
EDN, v43, n7, p18(2)
March 26, 1998
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 587 LINE COUNT: 00054

... process in a two-phase approach. The Flex10K "E" family goes a step beyond the EPF10K100B and improves the embedded-array-block (EAB) structure (see "**Programmable -logic** heavy-weights pack a punch," EDN Nov 20, 1997, pg 18). Doubling each EAB's density from 2 to 4 kbits, bus width from 8 to 16 bits, and number of I/O **ports** from **one** to **two** enables more efficient and higher performance FIFO and **dual -port** SRAM configurations. (Internet newsgroup comp.arch.fpga had criticized previous Flex10K devices for these oversights.) Altera predicts that the EPF10K100E, scheduled for sampling during the...

12/3,K/21 (Item 7 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09799229 SUPPLIER NUMBER: 19901708 (USE FORMAT 7 OR 9 FOR FULL TEXT)
/C O R R E C T I O N -- GateField/
PR Newswire, p1021SFTU063
Oct 21, 1997
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1058 LINE COUNT: 00098

... announced earlier this year. The GF250F family provides solutions for gate-intensive designs, whereas the GF260F family offers high density programmable memory in addition to **programmable logic** on a single chip.
This new product family is the industry's first and most flexible embedded memory solution in a non-volatile, yet reprogrammable ASIC technology and provides on a single chip 123,000 available gates and up to 46,000 bits of programmable memory optimized for **single -port** and **two -port** RAM as well as FIFO operation. Other programming options include multiple memories and FIFOs, synchronous or asynchronous operation and word width by word depth user...

12/3,K/22 (Item 8 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09149795 SUPPLIER NUMBER: 18914171 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Embedded memory enhances programmable logic for complex, compact designs.
Nelson, Rick
EDN, v41, n23, p91(9)
Nov 7, 1996
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2411 LINE COUNT: 00195

... one extreme (ILLUSTRATION FOR FIGURE 1 OMITTED). On the XC4000's "blank slate" of uncommitted logic blocks, you design your choice of synchronous or asynchronous, **single** - or **dual -port** memory, and logic functions, distributing each freely throughout the chip.
At the other extreme is the Wafer-Scale Integration Inc (WSI) PSD family (ILLUSTRATION FOR FIGURE 2 OMITTED). In addition to programmable **logic** , PSD devices include dedicated functions, such as interrupt controllers, counter/timers, EPROM, and RAM, carved in stone. The PSD devices are less PLDs with embedded memory than dedicated chips with some embedded field-**programmable logic** .
In fact, the WSI parts extend the capabilities of standard, off-the-shelf microcontrollers from such companies as Intel (Folsom, CA), Motorola (Austin, TX), and...
...PCI core on a PLD, but then I could sell it only to the PCI bus people, and that's never been the idea for **programmable logic** ." It doesn't make marketing sense for his company to pursue a niche with only 100 customers, he says: "The goal is a broad customer...

...company's CX2000 LPGAs provide 30,000 to 200,000 usable gates and as much as 128 kbits of 200-MHz SRAM, configurable as FIFO, **single -port** ,

or **dual -port** memory. An 80,000-gate device costs about $20 in very high volumes;

12/3,K/23 (Item 9 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08831464 SUPPLIER NUMBER: 18389500 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Lower-power and faster devices tackle multimedia needs.
Bursky, Dave
Electronic Design, v44, n9, p90(7)
May 1, 1996
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 4352 LINE COUNT: 00341

... assignments, while the compilation time can be measured in seconds. The basic chip consists of a central partial cross-bar, surrounded by alternating rows of **programmable** atomic **logic** elements (PALEs) and small crossbars (400 lines wide by 1600 lines deep) for connectivity between the PALE rows.

Also embedded on the chip are four 2-bit wide, 64-word deep register file blocks, each packing eight **read ports** and eight **write ports** (ILLUSTRATION FOR FIGURE 5B OMITTED). These register files can be concatenated to form a large register file.

To save on chip area, designers at HP...

12/3,K/24 (Item 1 from file: 553)
DIALOG(R)File 553:Wilson Bus. Abs. FullText

03773389 H.W. WILSON RECORD NUMBER: BWBA98023389 (USE FORMAT 7 FOR FULLTEXT)
Lucent rolls FPGA line, cuts prices.
AUGMENTED TITLE: Orca 2TxxA
Electronic News (New York, N.Y.: 1991) (Electron News (1991)) v. 44 (Feb. 2 '98) p. 25
LANGUAGE: English
WORD COUNT: 554

(USE FORMAT 7 FOR FULLTEXT)

...ABSTRACT: Microelectronics Group rolled out a four-layer metal, 0.25-micron family of field programmable gate arrays (FPGAs) designed to provide OEMs with high performance **programmable logic** devices while reducing the cost by in excess of 50 percent from previous process generations. The eight-device family, called the Orca 2TxxA, is intended to feature densities in the range of 15,000 to 40,000 real gates, four 16-bit look-up tables, eight three-state buffers, and **dual** or **single -port** asynchronous or synchronous SRAM operating at 96MHz. The family, which is a 3.3-volt series enabling most designers to effectively use it in current...

TEXT:
... 98 has rolled out a four-layer metal, 0.25-micron family of field programmable gate arrays (FPGAs) designed to provide OEMs with high performance **programmable logic** devices while reducing the cost by more than 50 percent from previous process generations.

The eight-device family, dubbed the Orca 2TxxA, is planned to feature densities in the range of 15,000 to 40,000 real gates, four 16-bit look-up tables, eight 3-state buffers, and **dual** or **single -port** asynchronous or synchronous SRAM operating at 96MHz. The family is a 3.3-volt series enabling most designers to effectively use the family in current...

...their primary driving force," said Mr. Britton. "With our roadmap to move down to smaller geometries I believe we will be able to supply the

programmable logic market with one of the highest performance families."
Along with the 0.25-micron family of FPGAs, Lucent is offering an additional speed grade improvement...

...full-burst core.
Added material
Lucent Technologies has introduced the Orca 2TxxA family of FPGAs featuring blocks of SRAM. Each FPGA in the family supports **dual** or **single -port** asynchronous or synchronous SRAM operating at 96MHz. Each block of SRAM can implement up to 128-bits of RAM.
...

12/3,K/25 (Item 1 from file: 9)
DIALOG(R)File 9:Business & Industry(R)

03163792 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Pulling the PLD market out of the doldrums
(Programmable logic market faces tough times; market size of global sales expected to decline to $4.7 bil in 2001 and increase to $10.8 bil in 2004)
EBN, p 61+
June 11, 2001
DOCUMENT TYPE: Journal ISSN: 0164-6362 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2904

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...in a family of Programmable Serial Interface (PSI) chips. The PSI2G100 combines one to eight 2.5Gbit/s serdes links with 100,000 gates of **programmable logic** for control functions. The device also adds 48Kbits of **dual -port** memory and 192Kbits of **single -port** RAM to support queuing and distributed switching. The primary target for this new device is InfiniBand and similar backplane networking applications.
"It's precision-tuned...

12/3,K/26 (Item 2 from file: 9)
DIALOG(R)File 9:Business & Industry(R)

02043091 (USE FORMAT 7 OR 9 FOR FULLTEXT)
New architectures & market targets -- Innovative programmable-logic designs are enabling the technology to encroach further on gate-arrays' turf
(Manufacturers of programmable logic devices are moving into the high-volume ASIC-replacement market)
Electronic Buyers News, p 03
January 19, 1998
DOCUMENT TYPE: Journal ISSN: 0164-6362 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2553

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...of implementing anything from fine-grained, three-input functions to coarse-grained, 16-input functions. The VF1 chip also features 200-MHz memory programmable for **one** - or **two -port** applications and a variable-length interconnect between sets of VGBs.

Development of the VF1 family grew out of ...its present generation. Design complexity increases with density. In some cases, the complexity of current-generation FPGAs threatens to undermine the rationale for moving to

programmable logic in the first place -- faster time to market.

"We found that if you're trying to implement designs into these larger 225K-gate FPGAs, your...

...Technologies Microelectronics Group, Berkeley Heights, N.J.

To deal with that dilemma, Lucent is working on additions to its Orca family of FPGAs, which combines **programmable logic** with mask-programmed logic on the same chip. The 5-V Orca 3C and 3.3-V Orca 3T series will range from 30K to...

...of the logic they use in a new design is based on some previous design," Britton said. "There's no use putting that in a **programmable -logic** piece, because you already know how it works. It makes more sense putting that in the fixed part of the mixed cell and focusing on...its new family of AT40K coprocessor FPGAs. Ranging in densities from 5K to 50K gates, the SRAM-based FPGAs feature distributed 10-ns synchronous/asynchronous, **dual -/single -port** SRAM.
Rather than trade off logic cells for SRAM or incorporate large SRAM blocks into the array as other FPGAs do, the AT40K places discrete...

12/3,K/27 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01238047 CMP ACCESSION NUMBER: EBN20010611S0045
Pulling The PLD Market Out Of The Doldrums - No one knows exactly when the recovery will begin, but PLD executives expect new technologies and applications, particularly in communications, to spur growth
John H. Mayer
EBN, 2001, n 1266, PG51
PUBLICATION DATE: 010611
JOURNAL CODE: EBN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: MARKET FOCUS
WORD COUNT: 2882

... in a family of Programmable Serial Interface (PSI) chips. The PSI2G100 combines one to eight 2.5Gbit/s serdes links with 100,000 gates of **programmable logic** for control functions. The device also adds 48Kbits of **dual -port** memory and 192Kbits of **single -port** RAM to support queuing and distributed switching. The primary target for this new device is InfiniBand and similar backplane networking applications.

"It's precision-

12/3,K/28 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01150447 CMP ACCESSION NUMBER: EBN19980119S0010
New architectures & market targets - Innovative programmable-logic designs are enabling the technology to encroach further on gate-arrays' turf
John H. Mayer
ELECTRONIC BUYER'S NEWS, 1998, n 1092, PG03
PUBLICATION DATE: 980119
JOURNAL CODE: EBN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News - Technology Focus: FPGAs and CPLDs
WORD COUNT: 2578

... of implementing anything from fine-grained, three-input functions to coarse-grained, 16-input functions. The VF1 chip also features 200-MHz

memory programmable for **one** - or **two** -**port** applications and a variable-length interconnect between sets of VGBs.

Development of the VF1 family grew out of a series of talks with current FPGA...its present generation.

Design complexity increases with density. In some cases, the complexity of current-generation FPGAs threatens to undermine the rationale for moving to **programmable logic** in the first place - faster time to market.

"We found that if you're trying to implement designs into these larger 225K-gate FPGAs, your...

...Technologies Microelectronics Group, Berkeley Heights, N.J.

To deal with that dilemma, Lucent is working on additions to its Orca family of FPGAs, which combines **programmable logic** with mask-programmed logic on the same chip. The 5-V Orca 3C and 3.3-V Orca 3T series will range from 30K to...

...of the logic they use in a new design is based on some previous design," Britton said. " There's no use putting that in a **programmable** - **logic** piece, because you already know how it works. It makes more sense putting that in the fixed part of the mixed cell and focusing on...its new family of AT40K coprocessor FPGAs. Ranging in densities from 5K to 50K gates, the SRAM-based FPGAs feature distributed 10-ns synchronous/ asynchronous, **dual** -/**single** -**port** SRAM.

Rather than trade off logic cells for SRAM or incorporate large SRAM blocks into the array as other FPGAs do, the AT40K places discrete...

12/3,K/29 (Item 1 from file: 813)
DIALOG(R)File 813:PR Newswire

1171587 SFTU063
In SFM101, "GateField Announces the First Embedded Memory ProASIC Family," moved yesterday, Oct. 20, the first graph, second line should read "(OTC: GATE)" rather than "(OTC Bulletin Board: GATE)" as incorrectly transmitted by PR Newswire. Complete corrected text follows.

DATE: October 21, 1997 14:10 EDT WORD COUNT: 938

... announced earlier this year. The GF250F family provides solutions for gate-intensive designs, whereas the GF260F family offers high density programmable memory in addition to **programmable logic** on a single chip.

This new product family is the industry's first and most flexible embedded memory solution in a non-volatile, yet reprogrammable ASIC technology and provides on a single chip 123,000 available gates and up to 46,000 bits of programmable memory optimized for **single** -**port** and **two** - **port** RAM as well as FIFO operation. Other programming options include multiple memories and FIFOs, synchronous or asynchronous operation and word width by word depth user...

12/3,K/30 (Item 2 from file: 813)
DIALOG(R)File 813:PR Newswire

1170864 SFM101
GateField Announces the First Embedded Memory ProASIC Family; New Family Offers Up to 310,000 Equivalent Gate Array Gates

DATE: October 20, 1997 17:42 EDT WORD COUNT: 940

... announced earlier this year. The GF250F family provides solutions for gate-intensive designs, whereas the GF260F family offers high density programmable memory in addition to **programmable logic** on a single chip.

This new product family is the industry's first and most flexible embedded memory solution in a non-volatile, yet reprogrammable ASIC technology and provides on a single chip 123,000 available gates and up to 46,000 bits of programmable memory optimized for **single -port** and **two - port** RAM as well as FIFO operation. Other programming options include multiple memories and FIFOs, synchronous or asynchronous operation and word width by word depth user...
?

17/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2001 The Gale Group. All rts. reserv.

02477308 SUPPLIER NUMBER: 69973482 (USE FORMAT 7 OR 9 FOR FULL TEXT)
9-Mbit SRAM supports 12 Gbits/second.
Electronic Engineering Times, 112
Feb 5, 2001
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 512 LINE COUNT: 00042

Strategic marketing manager Bill Beane said the new memory components are designed for applications in which two devices-microprocessors, digital signal processors, ASICs or **field -programmable gate** arrays, for example-can effectively share the same memory. A dual-port memory costs less, occupies less space and consumes less power than would dedicated **memory** configurations for each device.

Beane noted that two devices could share a common SRAM through a **single port** , but would have to take turns accessing the **memory** . IDT's **dual -port** architecture allows simultaneous **write** access from each device, albeit to different addresses, as well as simultaneous **read** access. Each **port** has its own control, address, clock and I/O pins. Designers can allocate as much of the memory as they wish to either device.

The...

17/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2001 The Gale Group. All rts. reserv.

02459462 SUPPLIER NUMBER: 67051011 (USE FORMAT 7 OR 9 FOR FULL TEXT)
EMBEDDED-PROCESSOR WORLD WAR : Action Heats Up on Multiple Fronts.(Company Business and Marketing)
Snyder, Cary D.
Microprocessor Report, 14, 10, 1
Oct, 2000
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2964 LINE COUNT: 00291

... widths in each family. To avoid wasting available die, the on-chip SRAM is scaled to match the size and number of pins in the **FPGA** . Excalibur devices scale the amount of **dual** - and **single -port** SRAM to the number of ports into the FPGA. Size options include 32KB, 128KB, and 256KB of **single -port** SRAM and 16KB, 64KB, and 128KB of **dual -port** SRAM. The number of ports into this **memory** scales with **two** , four, and eight **ports** . This creates a processor stripe with a fixed height and three lengths.

The size of the processor stripe in the 400K-gate EPXA4 and EPXM4...

17/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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02037298 SUPPLIER NUMBER: 19124696 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Chips: Xilinx begins shipping industry's largest FPGA device; company now sampling advanced 0.35 micron devices; ramps production of newest 5-volt products. (XC4062XL) (Product Announcement)
EDGE: Work-Group Computing Report, v8, p34(1)
Feb 10, 1997
DOCUMENT TYPE: Product Announcement LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 695 LINE COUNT: 00065

... be most like a gate-array."
Architectural Features Improve Device Performance, Utilization

Featuring identical architectures, the 3.3-volt XC4000XL and the 5-volt XC4000EX **FPGA** families permit each logic block to be configured as 32 bits of **single port** or 16 bits of **dual port** high-speed, synchronous **RAM** using the powerful Xilinx Select-**RAM** feature.

Select-**RAM** distributed **RAM** allows users ultimate flexibility in selecting the size and location of their RAM functions. The dual-port RAM makes the XC4000EX and XC4000XL devices ideal...

17/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01970868 SUPPLIER NUMBER: 18549453
Xilinx offers master interface PCI cores. (Company Business and Marketing)
Brown, Peter
Electronic News (1991), v42, n2127, p46(1)
July 29, 1996
ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 680 LINE COUNT: 00055

... said Mr. Balough.

A "select-RAM" feature of the XC4000E-2 includes the ability to select the size, function, location and programming method of the **FPGA** , and custom logic blocks (CLBs) allow designers to select either logic or **RAM** in their devices. The **RAM** functions of the device family can be **single** or **dual port** , synchronous or asynchronous; or designers can mix and match the two, according to Mr. Balough. The designer can select the location of the RAM anywhere...

17/3,K/5 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

02655198 Supplier Number: 65456991 (USE FORMAT 7 FOR FULLTEXT)
Cypress 4 Mbit Dual Port Memory Provides Density Upgrade For High-End Storage Networks, High-Speed WANs and Wireless Infrastructure Applications.
Business Wire, p2205
Sept 25, 2000
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 873

... bottlenecks, enabling more efficient backplane management and increasing overall system performance. Its low-power HSTL I/O provides an easy interface to common communications ICs, **CPLDs** , ASICs, and processors. The device will be manufactured using Cypress's **RAM7** (TM), fast transistor, 0.15-micron, CMOS process.

"The 4 Mbit **dual -port** establishes the upgrade path to higher densities for designers currently using Cypress's **1** Mbit **dual -port memories** ," said Chris Norris, Cypress's vice president, data communications division. "A growing number of designers rely on Cypress as the leader in dual-ported memories...

17/3,K/6 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01484191 Supplier Number: 47092893 (USE FORMAT 7 FOR FULLTEXT)
Xilinx Begins Shipping Industry's Largest FPGA Device; Company now sampling advanced 0.35 micron devices; ramps production of newest 5-volt products.
Business Wire, p02030018
Feb 3, 1997

Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 749

... be most like a gate-array."
Architectural Features Improve Device Performance, Utilization
Featuring identical architectures, the 3.3-volt XC4000XL and the 5-volt XC4000EX **FPGA** families permit each logic block to be configured as 32 bits of **single port** or 16 bits of **dual port** high-speed, synchronous **RAM** using the powerful Xilinx Select-**RAM** feature.
Select-**RAM** distributed **RAM** allows users ultimate flexibility in selecting the size and location of their RAM functions. The dual-port RAM makes the XC4000EX and XC4000XL devices ideal...

17/3,K/7 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03479041 Supplier Number: 47172847 (USE FORMAT 7 FOR FULLTEXT)
XILINX SAMPLING ADVANCED 0.35 MICRON DEVICES
Electro Manufacturing, v10, n3, pN/A
March 1, 1997
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 683

... be most like a gate-array."
Architectural Features Improve Device Performance, Utilization
Featuring identical architectures, the 3.3-volt XC4000XL and the 5-volt XC4000EX **FPGA** families permit each logic block to be configured as 32 bits of **single port** or 16 bits of **dual port** high-speed, synchronous **RAM** using the powerful Xilinx Select-**RAM** feature.
Select-**RAM** distributed **RAM** allows users ultimate flexibility in selecting the size and location of their RAM functions. The dual-port RAM makes the XC4000EX and XC4000XL devices ideal...

17/3,K/8 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03468716 Supplier Number: 47151629 (USE FORMAT 7 FOR FULLTEXT)
Xilinx Ships Largest FPGA Device
Semiconductor Industry & Business Survey, v19, n9, pN/A
Feb 24, 1997
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 196

... announced full production of the first two members of the XC4000EX family.
Featuring identical architectures, the 3.3-volt XC4000XL and the 5-volt XC4000EX **FPGA** families permit each logic block to be configured as 32 bits of **single port** or 16 bits of **dual port** high- speed, synchronous **RAM** using the powerful Xilinx Select-**RAM** feature.
Select-**RAM** allows flexibility in selecting the size and location of RAM functions. The dual-port RAM makes the XC4000EX and XC4000XL devices suitable for extremely high...

17/3,K/9 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03124735 Supplier Number: 46392584 (USE FORMAT 7 FOR FULLTEXT)

LUCENT TECHNOLOGIES INC: 0.35 micrometer ORCA ready for full production
M2 Presswire, pN/A
May 17, 1996
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 333

... enhancements to the original ORCA concept. New datapath modes enable frequently-used functions such as multipliers, comparators and multiplexers to operate faster, while occupying fewer **FPGA** resources. Extra features for **RAM** design allow the implementation of high-speed **single** - and **dual -port** synchronous **RAMs** . These new features support the trendtowards greater system hardware implementation within FPGAs.
Lucent's 0.35 micrometerm technology delivers a 30 percent speed increase over...

17/3,K/10 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04640126 Supplier Number: 46826218 (USE FORMAT 7 FOR FULLTEXT)
Orca FPGA software is Windows-compatible
Electronics Times, p30
Oct 24, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 167

The Orca families have datapath modes enabling frequently-used functions such as multipliers, comparators and multiplexers to operate faster, while occupying fewer **FPGA** resources. Extra features for **ram** design allow the implementation of high-speed, **single** and **dual -port** synchronous **rams** .
The Foundry 9.0 software provides third-party vendors with more libraries, as well as new back-annotation to VHDL and Verilog. A new trace ...

17/3,K/11 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04481533 Supplier Number: 46578906 (USE FORMAT 7 FOR FULLTEXT)
Xilinx Offers Master Interface PCI Cores
Electronic News (1991), p046
July 29, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 630

... said Mr. Balough.
A "select-RAM" feature of the XC4000E-2 includes the ability to select the size, function, location and programming method of the **FPGA** , and custom logic blocks (CLBs) allow designers to select either logic or **RAM** in their devices. The **RAM** functions of the device family can be **single** or **dual port** , synchronous or asynchronous; or designers can mix and match the two, according to Mr. Balough. The designer can select the location of the RAM anywhere...

17/3,K/12 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

13014869 SUPPLIER NUMBER: 20865393 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Flash-based field-programmable gate-array family adds 46 Kbits of SRAM. (static random access memory)
Bursky, Dave
Electronic Design, v45, n24, p68(2)
Nov 3, 1997
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 572 LINE COUNT: 00047

... support), or as a FIFO or other memory function. The memory blocks in the GF260F series, though, are the only blocks among all of the **FPGA** suppliers that have integrated FIFO support as well as parity generation and checking logic.

Multiport **memories** with independent, simultaneous read and write operations also can be configured - from one **read** and **write port** up to 10 **read** and **one write port** (multiple **writes** aren't supported). Access and cycle times for the **memory** are less than 15 ns, which allows the **memories** to deliver synchronous or asynchronous operation at speeds of up to 67 MHz, while consuming about 8 ((micro)watt)/gate/MHz.

There will initially be...

17/3,K/13 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

12822088 SUPPLIER NUMBER: 67326904 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Integrated Circuits.(Buyers Guide)
EDN, 45, 23, 191
Nov 9, 2000
DOCUMENT TYPE: Buyers Guide ISSN: 0012-7515 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 3748 LINE COUNT: 00335

... family, from less than $20 (10,000)
Quicklogic Corp, 1-408-990-4000, www.quicklogic.com
Enter No. 394 at www.rscahners.ims.ca/ednmag/
FPGAs
* Offer block **RAM** and high **memory** bandwidth
* XCV40SE packs 10,800 logic cells, 560 kbits of **dual -port** block **RAM**, and 404 maximum usable I/Os; XCV812E has 21,168 logic cells, more than 1 Mbit of **dual -port** block **RAM**, and 556 maximum usable I/Os
* XCV405E and XCV812E, $101 and $235 (50,000), respectively
Xilinx, 1-408-559-7778, www.xilinx.com
Enter No...

17/3,K/14 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

11851600 SUPPLIER NUMBER: 59834972 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Quad-Data-Rate SRAM Subsystems Maximize System Performance.
Rangasayee, Krishna; Manapat, Rajesh
Electronic Design, 48, 3, 117
Feb 7, 2000
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3143 LINE COUNT: 00235

... will interface a bank of four QDR chips. The chips are connected in a depth-expansion mode to a host CPU. A Xilinx Spartan-II **FPGA** will be used to implement the control logic for the memory interface (Fig. 3).

Each of the QDR SRAMs gets separate control signals for the **read** and **write ports**, while the address and data ports are common for all of the SRAMs. These SRAMs form a 2-Mword by 18-bit storage array. The controller generates all of the signals for the **memory** bank. It also supports concurrent DDR operations on all of the inputs and outputs, and

lets byte-write operations into the **memory** bank.

Operating in the single-dock mode, the controller really simplifies the **memory** interface. At 100 MHz, it provides a bandwidth of 7.2 Gbits/s. The controller employs a command-based interface with a 2-bit command... ...11 read/write) and has independent read and write state machines (Fig. 4). Those state machines are shown separately to simplify the understanding of the **memory** controller's operation. Each of their sections run in a pipelined fashion. The other inputs to the controller include clock (Clk), write address (Waddress), read...

...The state machine provides the addresses and data on certain clock edges, while the SRAM latches in the addresses and data on those edges. The **memory** controller looks at the command signal (Cmd) on its input port on every clock. Depending on that clock, either read, write, or read/write operations are completed on the bank of **memory** . The **memory** controller generates the **Read Port** Selects (RPSs) and **Write Port** Selects (WPSs) for the different SRAMs, depending on the state of the command (Cmd (0, 1)) inputs and the higher-order address lines.

Traditionally, designing...

17/3,K/15 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

11755650 SUPPLIER NUMBER: 55164946 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Special-purpose SRAMs smooth the ride.
Dipert, Brian
EDN, 44, 13, 93
June 24, 1999
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 4969 LINE COUNT: 00426

... control (analogous to the technique Motorola uses in its NetRAMs)?

For a long time, Lattice Semiconductor (www.latticesemi.com) with its ispLSI6192DM was the only **CPLD** manufacturer to offer on-chip **dual -port RAM** . Cypress Semiconductor now joins the party with its Delta39K family. Each 128-macrocell logic block contains **two** 8-kbit **single -port** SRAM arrays. An additional 4-kbit **dual -port** or FIFO block resides outside each logic block and directly connects to the hierarchical routing channels. The vendor's 39K100, for example, contains 240 kbits...

17/3,K/16 (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

10079624 SUPPLIER NUMBER: 20402746 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Programmable Logic -- Integrated Logic broadens its FPGA-to-ASIC conversion. (Integrated Logic Systems Inc) (Company Business and Marketing)
Cataldo, Anthony
Electronic Engineering Times, n998, p57(1)
March 16, 1998
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 439 LINE COUNT: 00036

... Hugh Chapman.

Higher logic density

New features incorporated into its MPGA-III include more-versatile I/O, increased logic density, dedicated delay cells for improved **FPGA** performance-matching and configurable **dual -port RAM** blocks.

MPGA-III contains **single** - and **dual -port RAM** organized in 32 x 18-bit blocks. Byte-write-enable makes it possible to configure the **RAM** in 64- x 9-bit blocks. RAM blocks are built under the routing channels so there is virtually no loss of available logic to use...

17/3,K/17 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2001 The Gale Group. All rts. reserv.

09781642 SUPPLIER NUMBER: 19847760 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Atmel's New AT40K Series FPGA Offers High Speed Computing and FreeRAM(TM)
PR Newswire, p1013SFM031
Oct 13, 1997
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1175 LINE COUNT: 00101

... compliant, dynamically reconfigurable AT40K Coprocessor FPGAs. Ranging in size from 5,000 to 50,000 usable gates, the 5-device AT40K family of SRAM-based **FPGAs** features distributed 10ns programmable synchronous/asynchronous, **dual port /single port** SRAM. The devices are supported by 8 global clocks, CacheLogic(R) ability (partially or fully reconfigurable without loss of data), and automatic component generators. I ...

...efficient, lowest cost FPGA for designs using SRAM. This is accomplished with Atmel's innovative, patented distributed 10ns SRAM capability, called "FreeRAM," which allows the **RAM** to be used without losing logic resources. Multiple independent, synchronous or asynchronous, **dual port** or **single port RAM** functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool. "Traditional FPGAs use logic cells for SRAM. For each block of...

17/3,K/18 (Item 1 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2001 Resp. DB Svcs. All rts. reserv.

02090287 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Programmable Logic -- Integrated Logic broadens its FPGA-to-ASIC conversion (Integrated Logic Systems Inc expands its service of converting FPGA and EPLD devices into gate-array ASICs with a new 0.5-micron CMOS triple-metal process for designs with up to 16,000 gates and 14 kbits of dual-port RAM)
Electronic Engineering Times, p 57
March 16, 1998
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 388

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...Hugh Chapman.

Higher logic density

New features incorporated into its MPGA-III include more-versatile I/O, increased logic density, dedicated delay cells for improved **FPGA** performance-matching and configurable **dual -port RAM** blocks.

MPGA-III contains **single** - and **dual -port RAM** organized in 32 x 18-bit blocks. Byte-write-enable makes it possible to configure the **RAM** in 64- x 9-bit blocks. RAM blocks are built under the routing channels so there is virtually no loss of available logic to use...

17/3,K/19 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2001 CMP. All rts. reserv.

01231049 CMP ACCESSION NUMBER: EET20010205S0089
9-Mbit SRAM supports 12 Gbits/second
ELECTRONIC ENGINEERING TIMES, 2001, n 1152, PG112
PUBLICATION DATE: 010205
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: PRODUCTWEEK - CHIPS
WORD COUNT: 464

Strategic marketing manager Bill Beane said the new memory components are designed for applications in which two devices- microprocessors, digital signal processors, ASICs or **field - programmable gate** arrays, for example-can effectively share the same memory. A dual-port memory costs less, occupies less space and consumes less power than would dedicated **memory** configurations for each device.

Beane noted that two devices could share a common SRAM through a **single port** , but would have to take turns accessing the **memory** . IDT's **dual -port** architecture allows simultaneous **write** access from each device, albeit to different addresses, as well as simultaneous **read** access. Each **port** has its own control, address, clock and I/O pins. Designers can allocate as much of the memory as they wish to either device.

The...

17/3,K/20 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01155649 CMP ACCESSION NUMBER: EET19980316S0060
Programmable Logic - Integrated Logic broadens its FPGA-to -ASIC conversion
Anthony Cataldo
ELECTRONIC ENGINEERING TIMES, 1998, n 998, PG57
PUBLICATION DATE: 980316
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design
WORD COUNT: 396

... Hugh Chapman.
Higher logic density
New features incorporated into its MPGA-III include more-versatile I/O, increased logic density, dedicated delay cells for improved **FPGA** performance-matching and configurable **dual -port RAM** blocks.
MPGA-III contains **single** - and **dual -port RAM** organized in 32 x 18- bit blocks. Byte-write-enable makes it possible to configure the **RAM** in 64- x 9-bit blocks. RAM blocks are built under the routing channels so there is virtually no loss of available logic to use...
?

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File 347:JAPIO OCT 1976-2001/Feb(UPDATED 010604)
        (c) 2001 JPO & JAPIO
File 350:Derwent WPIX 1963-2001/UD,UM &UP=200136
        (c) 2001 Derwent Info Ltd

Set     Items   Description
S1       4445   PROGRAMMABLE(1W)LOGIC?
S2       1384   SPLD? ? OR CPLD? ? OR FPGA? ? OR FPIC? ? OR FIELD()PROGRAM-
            MABLE()(GATE? ? OR INTERCONNECT? ? OR INTER()CONNECT? ?)
S3      65751   LOGIC?(2W)(UNIT? ? OR DEVICE? ? OR CIRCUIT?? OR MICROCIRCU-
            IT? ? OR CHIP? ? OR MODULE? ? OR BOARD? ? OR BLOCK? ? OR MICR-
            OCHIP? ? OR IC OR APPARATUS)
S4     800944   RAM OR MEMOR???
S5       2706   READ?(5N)PORT? ?
S6       1537   WRIT???(5N)PORT? ?
S7      47112   SINGLEPORT? ? OR (SINGLE OR ONE OR 1)(5N)PORT? ?
S8      48054   DUALPORT? ? OR (DUAL OR TWO OR 2 OR MULTIPLE OR DUAL OR SE-
            CONDARY OR SEPARATE OR DIFFERENT OR TWIN)(5N)PORT? ?
S9         35   S1 AND S8
S10        25   S4 AND S9
S11         5   S10 AND S7
S12         6   S1 AND S4 AND S5 AND S6
S13        10   S11:S12
S14        33   S2:S3 AND S4 AND S5 AND S6
S15        43   S2:S3 AND S4 AND S7 AND S8
S16        68   S14:S15
S17     95239   IC=(H03K-007 OR H03K-019 OR G06F-007 OR G11C-007 OR G11C-0-
            08)
S18        31   S16 AND S17
S19        25   S18 NOT S13
S20     18601   MULTIPORT? ? OR (DOUBLE OR MULTI OR SECOND?)(5N)PORT? ?
S21        13   S1:S3 AND S4 AND S7 AND S20
S22         5   S21 NOT (S13 OR S19)
S23        20   S1:S3 AND S5 AND S6 AND S17
S24        31   S1:S3 AND S7 AND (S8 OR S20) AND S17
S25        12   S23:S24 NOT (S13 OR S19 OR S22)
S26         5   AU="NGAI T"
S27       141   AU="PATEL R" OR AU="PATEL R H"
S28        63   AU="REDDY S" OR AU="REDDY S T" OR AU="REDDY SRINIVAS T"
S29        80   AU="CLIFF R" OR AU="CLIFF R G" OR AU="CLIFF RICHARD G"
S30         6   S26:S29 AND S1:S3 AND PORT? ?
```

13/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2001 Derwent Info Ltd. All rts. reserv.

013780904 **Image available**
WPI Acc No: 2001-265115/200127
XRPX Acc No: N01-189544
Logic cell of programmable logic **device, has random access** memory **which includes circuitry adapted to selectively choose between several** memory **configurations among** single port memories **and** dual port memories
Patent Assignee: XILINX INC (XILI-N)
Inventor: SASAKI P T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6198304	B1	20010306	US 9875784	A	19980223	200127	B
			US 99255237	A	19990222		

Priority Applications (No Type Date): US 9875784 A 19980223; US 99255237 A 19990222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6198304	B1		25	G06F-007/38	Provisional application US 9875784

Abstract (Basic): US 6198304 B1
NOVELTY - A random access **memory** (200) includes a circuitry which is adapted to selectively choose between several **memory** configuration selected from a set consisting of **single port** random access **memory** and **dual port memory** .
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method for operating logic cell.
USE - For **programmable logic** device e.g. PLA, field programmable gate array (FPGA).
ADVANTAGE - Increases functional flexibility of logic cell. Allows augmentation of overall efficiency of logic cell.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic drawing of the circuitry of one logic cell employing a **RAM** element.
Random access **memory** (200)
pp; 25 DwgNo 3/10
Title Terms: LOGIC; CELL; PROGRAM; LOGIC; DEVICE; RANDOM; ACCESS; **MEMORY** ; CIRCUIT; ADAPT; SELECT; CHOICE; **MEMORY** ; CONFIGURATION; SINGLE; PORT; **MEMORY** ; DUAL; PORT; **MEMORY**
Derwent Class: T01; U21
International Patent Class (Main): G06F-007/38
File Segment: EPI

13/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2001 Derwent Info Ltd. All rts. reserv.

013772030 **Image available**
WPI Acc No: 2001-256241/200126
XRPX Acc No: N01-182625
Programmable logic **device has** two **sets of combinable** single port memory **arrays that are combined to form** dual port memory **arrays, are arranged in intersecting rows and columns**
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: LANE C F; MEJIA M; REDDY S T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6191998	B1	20010220	US 9761983	A	19971016	200126	B
			US 98107926	A	19980630		
			US 99452627	A	19991201		

Priority Applications (No Type Date): US 9761983 A 19971016; US 98107926 A 19980630; US 99452627 A 19991201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6191998	B1		21	G11C-008/00	Provisional application US 9761983 CIP of application US 98107926

Abstract (Basic): US 6191998 B1

NOVELTY - **Programmable logic** regions (88) and **two** sets of combinable **single port memory** arrays (84) are arranged in intersecting rows and columns. Each set of **memory** arrays (84) associated with other set, has rows and columns of **memory** cells to store data. Two sets of array (84) are combined to form **dual port memory** arrays. Interconnects (90,92) are provided to route signals between logic region and **memory** array.

USE - In **programmable logic** device **memory** arrays that consists of EPROM, EEPROM, **RAM** , transistors.

ADVANTAGE - Since each set of combinable **single port memory** arrays are used individually, logic resources are not wasted when **dual port** function of **memory** array circuit is not needed.

DESCRIPTION OF DRAWING(S) - The figure shows the **programmable logic** device.

Single port memory arrays (84)
Programmable logic regions (88)
Interconnects (90,92)
pp; 21 DwgNo 5/9

Title Terms: PROGRAM; LOGIC; DEVICE; TWO; SET; COMBINATION; SINGLE; PORT; **MEMORY** ; ARRAY; COMBINATION; FORM; DUAL; PORT; **MEMORY** ; ARRAY; ARRANGE; INTERSECT; ROW; COLUMN
Derwent Class: U13; U14
International Patent Class (Main): G11C-008/00
International Patent Class (Additional): G11C-007/00
File Segment: EPI

13/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012987985 **Image available**
WPI Acc No: 2000-159838/200014
Related WPI Acc No: 2000-159829; 2001-217310
XRPX Acc No: N00-119259
Multi-port memory **block for field** programmable logic **array**
Patent Assignee: ALTERA CORP (ALTE-N); QUICKTURN DESIGN SYSTEMS INC (QUIC-N)
Inventor: BUTTS M R; CHEN C C; NORMAN K A; PATEL R H; SAMPLE S P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6011744	A	20000104	US 97895516	A	19970716	200014	B

Priority Applications (No Type Date): US 97895516 A 19970716
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6011744	A		14	G11C-008/00	

Abstract (Basic): US 6011744 A

NOVELTY - The **memory** block (10) comprises a **read port** (12) that **reads** data out of the **memory** block. A **write port** (16) **writes** data into the **memory** block. The width and depth of the **read port** is independent of the **write port** .

DETAILED DESCRIPTION - The block has **memory** cells with configurable width and depth such that increasing the width results in decreasing the depth and decreasing the width results in increasing the depth.

USE - For a field **programmable logic** array.
ADVANTAGE - Enables implementing reconfigurable logic having a **memory** whose width and depth are configurable in a trade-off fashion.
DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the **memory** block.
Memory block (10)
Read port (12)
Write port (16)
pp; 14 DwgNo 1/11
Title Terms: MULTI; PORT; **MEMORY** ; BLOCK; FIELD; PROGRAM; LOGIC; ARRAY
Derwent Class: U13; U14
International Patent Class (Main): G11C-008/00
File Segment: EPI

13/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012422602 **Image available**
WPI Acc No: 1999-228710/199919
Related WPI Acc No: 1998-479951; 2001-225825
XRPX Acc No: N99-169203
Composable RAM **array for** programmable logic **device (PLD)**
Patent Assignee: XILINX INC (XILI-N)
Inventor: NEW B J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5886538	A	19990323	US 96631298	A	19960409	199919	B
			US 98104465	A	19980625		

Priority Applications (No Type Date): US 96631298 A 19960409; US 98104465 A 19980625
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5886538	A		16	H03K-007/38	Cont of application US 96631298 Cont of patent US 5796269

Abstract (Basic): US 5886538 A
NOVELTY - **Memory** tiles (302) having array of **single** or **dual port RAM** cells (MC0-MC127) with **one port** coupled to a bit line (541,542) are provided. A configuration circuit is programmable to establish or break the continuity of bit lines. A dedicated decoder accesses the array of **RAM** cells.
USE - For PLD.
ADVANTAGE - Any number of consecutive **memory** tiles can be concatenated to form a **memory** array using the configuration circuits and bit lines. By controlling the length of the bit lines, the size of the resulting **memory** array is controlled. The configuration circuits also allow the composable **RAM** array to be divided into separate **memories** .
DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of **memory** tile.
Memory tile (302)
Bit line (541,542)
Dual port SRAM cells (MC0-MC127)
pp; 16 DwgNo 4a/8
Title Terms: **RAM** ; ARRAY; PROGRAM; LOGIC; DEVICE
Derwent Class: U21; U22
International Patent Class (Main): H03K-007/38
File Segment: EPI

13/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011505378 **Image available**
WPI Acc No: 1997-483292/199745
XRPX Acc No: N97-402849

Configurable logic block in programmable logic **device integrated circuit - has local interconnect with number of conductors which are programmably coupled to** memory **array, first and second registers**

Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: VEENSTRA K S

Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2312305	A	19971022	GB 977548	A	19970415	199745 B
US 5977791	A	19991102	US 9615443	A	19960415	199953
			US 97834426	A	19970414	
GB 2312305	B	20000906	GB 977548	A	19970415	200044
US 6242946	B1	20010605	US 9615443	A	19960415	200133
			US 97834426	A	19970414	
			US 99369409	A	19990805	

Priority Applications (No Type Date): US 9615443 A 19960415; US 97834426 A 19970414; US 99369409 A 19990805
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2312305	A		33	H03K-019/177	
US 5977791	A			H03K-019/177	Provisional application US 9615443
GB 2312305	B			H03K-019/177	
US 6242946	B1			H03K-019/177	Provisional application US 9615443 Cont of application US 97834426 Cont of patent US 5977791

Abstract (Basic): GB 2312305 A

The logic block includes a **memory** array (650), having a number of **memory** cells arranged in a **RAM** format and address lines to uniquely address each of the number of **memory** cells. A first register (640) is coupled to the address lines of the **memory** array. In a FIFO mode the configurable logic block operates as a first-in, first-out **memory** and the first register contains a write address, while a second register (630) is coupled to the address lines of the **memory** array. In the FIFO mode, the second register contains a read address. A local interconnect has a number of conductors which are programmably coupled to the **memory** array, the first register, and the second register.

In the FIFO mode, the first and second registers are configured as a counter. The address lines of the **memory** array further comprise a **write** address **port** that is coupled to the first register when in the FIFO mode. A **read** address **port** is coupled to the second register when in the FIFO mode.

ADVANTAGE - Allows implementation of FIFO **memory** while saving programmable interconnect lines.

Dwg.6/10

Title Terms: CONFIGURATION; LOGIC; BLOCK; PROGRAM; LOGIC; DEVICE; INTEGRATE ; CIRCUIT; LOCAL; INTERCONNECT; NUMBER; CONDUCTOR; PROGRAM; COUPLE; **MEMORY** ; ARRAY; FIRST; SECOND; REGISTER
Derwent Class: U13; U14; U21
International Patent Class (Main): H03K-019/177
File Segment: EPI

13/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010967507 **Image available**
WPI Acc No: 1996-464456/199646
Related WPI Acc No: 1995-320154

XRPX Acc No: N96-391198
Multi-port memory **circuit implementing method for** programmable logic **device - involves tagging** memory **location of each of** read- port memory **arrays located within one of Z** write- port memory **arrays is tagged as "last written" when data is written to that** memory **location**
Patent Assignee: QUICKTURN DESIGN SYSTEMS INC (QUIC-N)
Inventor: HUANG T B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5563829	A	19961008	US 94217049	A	19940324	199646	B
			US 95522865	A	19950901		

Priority Applications (No Type Date): US 94217049 A 19940324; US 95522865 A 19950901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5563829	A		16	G11C-013/00	Cont of application US 94217049 Cont of patent US 5448522

Abstract (Basic): US 5563829 A
The method involves creating Z **write -port memory** arrays. Each of the Z **write -port memory** arrays includes Y **read -port memory** arrays. Each of the Y **read -port memory** arrays comprise a duplication of the **memory** array. Each respective Y **read -port memory** arrays of each respective of the Z **write -port memory** arrays is placed in communication with one of a respective correspond ing Y multiplexers. The **memory** location of each of the **read -port memory** arrays located within one of the Z **write -port memory** arrays is tagged as ''last written'' when data is written to that **memory** location.
ADVANTAGE - Does not require large number of configurable logic blocks.
Dwg.3/6
Title Terms: MULTI; PORT; **MEMORY** ; CIRCUIT; IMPLEMENT; METHOD; PROGRAM; LOGIC; DEVICE; TAG; **MEMORY** ; LOCATE; READ; PORT; **MEMORY** ; ARRAY; LOCATE ; ONE; WRITING; PORT; **MEMORY** ; ARRAY; TAG; LAST; WRITING; DATA; WRITING; **MEMORY** ; LOCATE
Derwent Class: U14
International Patent Class (Main): G11C-013/00
File Segment: EPI

13/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2001 Derwent Info Ltd. All rts. reserv.

010452072 **Image available**
WPI Acc No: 1995-353390/199546
XRPX Acc No: N95-263547
Monitoring appts. e.g. for robot, numerical control appts., in assembly line of plant - has two CPUs for processing programmable devices read from programmable logic **controller and returning result to** two- port memory, **and for** reading **result from** memory **and displaying it on CRT**
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: IKENO T; KATO H; SHIKIDA H; TAKAI S
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2288674	A	19951025	GB 956585	A	19950330	199546	B
DE 19512194	A1	19951221	DE 1012194	A	19950331	199605	
JP 7319511	A	19951208	JP 9566444	A	19950324	199607	
US 5615104	A	19970325	US 95413640	A	19950330	199718	
GB 2288674	B	19980422	GB 956585	A	19950330	199818	

TW 367454 A 19990821 TW 94104314 A 19940513 200033
Priority Applications (No Type Date): JP 9566444 A 19950324; JP 9463035 A 19940331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2288674	A		122	G05B-023/02	
DE 19512194	A1		69	G05B-019/048	
JP 7319511	A		28	G05B-019/048	
US 5615104	A		64	G05B-015/00	
GB 2288674	B			G05B-023/02	
TW 367454	A			G06F-015/62	

Abstract (Basic): GB 2288674 A

The appts. comprises a first processor which reads, from a first **memory** in which a predetermined number of screen data representing a screen display for displaying on a display unit are stored, a predetermined number of addresses of the device **memory** , which are described in the predetermined number of screen data, and writes the predetermined number oa addresses to a **two -port memory** . A second processor sends each of the predetermined number of addresses **written** in the **two -port memory** to at least **one** of the programmable controllers, reads the contents at each of the addresses of the device **memory** from the at least one programmable controller, and **writes** , to the **two -port memory** , the contents **read** or a result obtained by performing predetermined calculations on the read contents.

The first processor further executes display processes for displaying a screen display on the display device based on the predetermined number of screen data, reads, based on the predetermined number of screen data, parts of the contents **written** in the second-**port memory** by said second processor, which are necessary for screen display based on the predetermined number of screen data, and executes a display process to display the read parts of the contents. The first and second processors perform their respective operations at the same time independently of each other.

ADVANTAGE - Enables monitor display, which displays the operation of the programmable device, to have a fast response time. Is capable of obtaining log file data while trends are being displayed at intervals of one second.

Dwg.1/5

Title Terms: MONITOR; APPARATUS; ROBOT; NUMERIC; CONTROL; APPARATUS; ASSEMBLE; LINE; PLANT; TWO; CPU; PROCESS; PROGRAM; DEVICE; READ; PROGRAM; LOGIC; CONTROL; RETURN; RESULT; TWO; PORT; **MEMORY** ; READ; RESULT; **MEMORY** ; DISPLAY; CRT
Index Terms/Additional Words: **PLC_CE NTRAL_** ; CENTRAL; PROCESSING; UNIT
Derwent Class: T01; T06; X25
International Patent Class (Main): G05B-015/00; G05B-019/048; G05B-023/02; G06F-015/62
International Patent Class (Additional): G05B-019/02; G05B-019/05; G05B-019/18
File Segment: EPI

13/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010418839 **Image available**
WPI Acc No: 1995-320154/199541
Related WPI Acc No: 1996-464456
XRPX Acc No: N95-240850

Programmable logic **device multi-port** memory **implementation method - involves implementing** memory **resources to define** read- port memory **array which is duplicated to define** write- port memory **which is also duplicated and implementing** memory **registering TAG array**

Patent Assignee: QUICKTURN DESIGN SYSTEMS INC (QUIC-N)
Inventor: HUANG T B

Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5448522	A	19950905	US 94217049	A	19940324	199541	B
GB 2287810	A	19950927	GB 955638	A	19950321	199542	
DE 19510902	A1	19950928	DE 1010902	A	19950324	199544	
FR 2717923	A1	19950929	FR 953507	A	19950324	199544	
JP 8044787	A	19960216	JP 9566549	A	19950324	199617	
GB 2287810	B	19980729	GB 955638	A	19950321	199832	

Priority Applications (No Type Date): US 94217049 A 19940324
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5448522	A		16	G11C-013/00	
GB 2287810	A		35	G11C-007/00	
DE 19510902	A1		17	G06F-017/50	
JP 8044787	A		13	G06F-017/50	
FR 2717923	A1			G06F-017/60	
GB 2287810	B			G11C-007/00	

Abstract (Basic): US 5448522 A

The method involves using **memory** resources and logic resources of the **programmable logic** device, e.g. an FPGA. The **memory** locations in the **memory** resources are implemented (1300) to define a **read -port memory** array. The **read -port memory** array is then duplicated (1400) in the **memory** resources for each of the **read ports** of the multi-**port memory** circuit. This acts to define a **write -port memory** array having a number of **read -port memory** arrays being equal to the number of **read ports** of the multi-**port memory** circuit.

The **write -port memory** array is then also duplicated (1500) in the **memory** resources for each of the **write ports** of the multi-**port memory** circuit. A TAG array having a register for each of the **memory** locations located within each **write -port memory** array is finally implemented (1200). The register stores data indicative of whether the **memory** location corresponding to that register ''last written'' data inside it.

ADVANTAGE - **Memory** arrays are tagged to indicate which **memory** location had data written to it last so that only last written data will be **read** through various **read ports** . Emulates multi-**port memory** circuits without requiring large number of configurable logic blocks.

Dwg.3/6

Title Terms: PROGRAM; LOGIC; DEVICE; MULTI; PORT; **MEMORY** ; IMPLEMENT; METHOD; IMPLEMENT; **MEMORY** ; RESOURCE; DEFINE; READ; PORT; **MEMORY** ; ARRAY; DUPLICATE; DEFINE; WRITING; PORT; **MEMORY** ; DUPLICATE; IMPLEMENT; **MEMORY** ; REGISTER; TAG; ARRAY
Index Terms/Additional Words: **FIELD** ; **PROGRAMMABLE** ; **GATE** ; **ARRAY**
Derwent Class: U14
International Patent Class (Main): G06F-017/50; G06F-017/60; G11C-007/00; G11C-013/00
International Patent Class (Additional): G06F-009/455; G06F-012/00; G11C-011/401
File Segment: EPI

13/5/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008462979 **Image available**
WPI Acc No: 1990-349979/199047
XRPX Acc No: N90-267352
Noncacheable address random access memory **- has processor, cache** memory **controller and store for data values representing** memory **block cacheable status**

Patent Assignee: COMPAQ COMPUTER CORP (COPQ)
Inventor: BRASHER G L; CULLEY R R; NUCKOLS J H; THOME G W; BRASHER G; CULLEY R; NUCKOLS J; CULLEY P R
Number of Countries: 013 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 398189	A	19901122	EP 90108940	A	19900511	199047	B
CA 2016544	A	19901119				199107	
US 5210847	A	19930511	US 89354513	A	19890519	199320	
EP 398189	B1	19970305	EP 90108940	A	19900511	199714	
DE 69030022	E	19970410	DE 630022	A	19900511	199720	
			EP 90108940	A	19900511		

Priority Applications (No Type Date): US 89354513 A 19890519
Cited Patents: 1.Jnl.Ref; A3...9143; EP 200440; EP 309995; NoSR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 398189	A				
Designated States (Regional): BE CH DE ES FR GB GR IT LI NL SE					
US 5210847	A		10	G06F-012/06	
EP 398189	B1	E	11	G06F-012/08	
Designated States (Regional): BE CH DE ES FR GB GR IT LI NL SE					
DE 69030022	E			G06F-012/08	Based on patent EP 398189

Abstract (Basic): EP 398189 A

The computer system utilises random access **memory** (**RAM**) to perform the decoding function for noncacheable addresses. The **RAM** is connected with its address inputs connected to the address bus and with a data output coupled to the cache controller's non-cacheable address input. When a given address is requested by the microprocessor, the **RAM** outputs a value indicative of the cacheability of that **memory** block. Because a **RAM** is being utilised each **memory** block can be individually programmed to a proper condition, thus removing the restrictions of the PAL and allowing small users or special applications to have a correctly configured cacheability map.

The **RAM** is initially loaded during power on self test (POST) operations and can be read or modified at other times. Writing to the **RAM** is accomplished by setting the desired data value, a write flag and a programming value by performing an input/output (I/O) **write** operation to an I/O **port** associated with the circuitry of the present invention. The I/O **port** is **read** to insure that the I/O write operation is complete. A **memory** write operation to the desired **memory** block completes the sequence. The **memory** write operation is done in a local bus access mode so that the main **memory** of the system is not affected. This process is repeated for all the **memory** blocks to insure that the proper values are present in the **RAM** .

ADVANTAGE - Fast, inexpensive. (15pp Dwg.No.1/4

Title Terms: ADDRESS; RANDOM; ACCESS; **MEMORY** ; PROCESSOR; CACHE; **MEMORY** ; CONTROL; STORAGE; DATA; VALUE; REPRESENT; **MEMORY** ; BLOCK; STATUS
Derwent Class: T01
International Patent Class (Main): G06F-012/06; G06F-012/08
International Patent Class (Additional): G06F-013/00
File Segment: EPI

13/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004019545
WPI Acc No: 1984-165087/198426
XRPX Acc No: N84-122886
High speed LSI CMOS-SOS programmable **arithmetic** logic **unit - has all operations programmable and performed simultaneously in one clock period**
Patent Assignee: US SEC OF AIR FORCE (USAF)
Inventor: MILLER G I

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4454589	A	19840612	US 82357440	A	19820312	198426	B

Priority Applications (No Type Date): US 82357440 A 19820312
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4454589	A		4		

Abstract (Basic): US 4454589 A

The unit performs high speed bit sliced, pipelined computations at low power and is microprogrammable. The device operates in conjunction with a fast microgram store program **memory** and controller. **Dual** input **ports** which supply data from eight sources are latched and operated on while new data is simultaneously fetched.

Instruction bits shift data in either port left or right, select complements and select an operand between device input and output data in **one** **port** . The data processed in each port is compared and is added to provide a latched tri-state output to an external device. The device comprises input, operand select and shift multiplexers and a latch strobed by a clock for the output of the first multiplexer. A complement select multiplexer, a second input multiplexer and an adder are also included.

0/1

Title Terms: HIGH; SPEED; LSI; CMOS; SOS; PROGRAM; ARITHMETIC; LOGIC; UNIT; OPERATE; PROGRAM; PERFORMANCE; SIMULTANEOUS; ONE; CLOCK; PERIOD
Index Terms/Additional Words: SILICON; SAPPHIRE
Derwent Class: T01
International Patent Class (Additional): G06F-007/50; H03K-019/20
File Segment: EPI

19/TI/1 (Item 1 from file: 347)
DIALOG(R)File 347:(c) 2001 JPO & JAPIO. All rts. reserv.

DIGITAL **LOGIC CIRCUIT**

19/TI/2 (Item 2 from file: 347)
DIALOG(R)File 347:(c) 2001 JPO & JAPIO. All rts. reserv.

MEMORY APPLYING CIRCUIT

19/TI/3 (Item 3 from file: 347)
DIALOG(R)File 347:(c) 2001 JPO & JAPIO. All rts. reserv.

PROCESSOR

19/TI/4 (Item 1 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Simultaneous read or write memory **array for portable computer, cellular telephone, has bit lines of ports connected to** memory **array whose control inputs are coupled to control logic inputs**

19/TI/5 (Item 2 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

High speed synchronous write control unit for semiconductor memory **sets time cycle of write data transferred to data lines, to be still active at same point as that during read**

19/TI/6 (Item 3 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Dual-ported static RAM **block**

19/TI/7 (Item 4 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Random access memory **apparatus**

19/TI/8 (Item 5 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Configurable static random access memory **(SRAM) for** field programmable gate **array (FPGA)**

19/TI/9 (Item 6 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Fuzzy logic circuit **e.g. for vacuum cleaner - adds membership function selection signal to subtraction of crisp input and centre data, outputs as address to** memory, **which sends attachment degree 5-bit segments via multiplexer to AND-gate**

19/TI/10 (Item 7 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Dual port memory **appts. for portable computer e.g. notebook**

personal computer - has serial counter synchronised with standard clock that provides address value to data serially generated from RAM **I/O buffer to SAM I/O buffer**

19/TI/11 (Item 8 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Field programmable gate **array with multi-port** RAM **- has look-up table for implementing number of functions including** RAM **cells and programmable switching device for coupling and decoupling** RAM **cells**

19/TI/12 (Item 9 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Pattern recognition appts. for computation and logic units **- has parallel functioning arithmetic logic pipelines coupled to** memory **storage area, pointer pipelines supplying operands from** memory, **multiplexer selecting positive result**

19/TI/13 (Item 10 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Double port memory **switching matrix utilised as FIFO device for ATM communication network - has** single **buffered** write port **and** read port **for each** memory **of matrix with separate address and control signals**

19/TI/14 (Item 11 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Configurable logic element capable of logic and arithmetic operation - provides multifunction use of memory **cells by organising cells in** memory **banks and by providing internal configurable interconnections**

19/TI/15 (Item 12 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Arithmetic unit for structure arithmetic processing in computers - controls storage registers according to list instructions belonging to lists stored in registers

19/TI/16 (Item 13 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Collision detection system for multiport memory **- has match signal which controls forward** logic circuit **which connects** write port **to** read port

19/TI/17 (Item 14 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Semiconductor storage device with common data line - has 2 switch MOSFET'S coupled between data line and terminal supplied with power source voltage level, e.g. ground potential

19/TI/18 (Item 15 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Semiconductor memory **e.g. multiport** memory **in gate array integrated circuit - has data selector to allow data by-pass** memory **cell array when addresses defined by read and** write ports **agree**

19/TI/19 (Item 16 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Digital signal processor with five-stage pipeline - has three internal data buses interfaced with dual port **internal** memory **and arithmetic unit and with external** memory **through interface**

19/TI/20 (Item 17 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Dual port memory **word size expansion - has master chip providing signal from conflict resolution circuitry to slave chips to prevent selection of opposite ports**

19/TI/21 (Item 18 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Multifunctional sequential logic circuit **- uses** dual- port RAM **with function defining means to allow for function modification**

19/TI/22 (Item 19 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Microprocessor instruction pre-fetch buffer - is organised as one- port - write, **two-** port- read memory **array in which instruction are accessed on instruction boundaries**

19/TI/23 (Item 20 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Integrated circuit memory **system - uses multiple sub-arrays of** memory **with simultaneous execution of range of functions**

19/TI/24 (Item 21 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

High-speed digital data processor system for vectors - uses two **CPUS connected by** ports **to access paths of central** memory, **and shared registers connected to internal information paths of CPU**

19/TI/25 (Item 22 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Data path configuration for data processing system - includes CUP operating asynchronously with ROM units enabling independent operation
?

19/5/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012408184 **Image available**
WPI Acc No: 1999-214292/199918
XRPX Acc No: N99-157695
Configurable static random access memory **(SRAM) for** field programmable gate **array (FPGA)**
Patent Assignee: DYNACHIP CORP (DYNA-N)
Inventor: GHIA A V; SASAKI P T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5883852	A	19990316	US 9828956	A	19980223	199918	B

Priority Applications (No Type Date): US 9828956 A 19980223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5883852	A		14	G11C-008/00	

Abstract (Basic): US 5883852 A
NOVELTY - Two steering signal inputs, a x1/x2 steering signal input, a **dual port /single port** signal input and the inputs and outputs of two **memory** arrays (50,52) are selectively connected to appropriate data, address and write enable signal inputs to establish selectability between an N x2 **single** port configuration, a 2N x1 **single port** configuration or a 2N x1 **dual port** configuration.
DETAILED DESCRIPTION - N is the number of bits stored in each of the **memory** arrays. INDEPENDENT CLAIMS are included for a subsystem apparatus of a configurable **memory** array.
USE - For **FPGAs** .
ADVANTAGE - Can be switched between **dual port** and **single port** configurations. Can be either a x1 configuration where all cells are unified in a single **memory** or a x2 configuration where the cells available are split into **two** separate RAMs, each **single port** and with its own input/output address and data inputs and data output.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic diagram of the configurable **memory** system as configured for 32 x1 **dual port** operation.
memory arrays (50,52)
pp; 14 DwgNo 2/7
Title Terms: CONFIGURATION; STATIC; RANDOM; ACCESS; **MEMORY** ; SRAM; FIELD; PROGRAM; GATE; ARRAY
Derwent Class: U13; U14
International Patent Class (Main): **G11C-008/00**
International Patent Class (Additional): G11C-016/04
File Segment: EPI

19/5/11 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2001 Derwent Info Ltd. All rts. reserv.

010945595 **Image available**
WPI Acc No: 1996-442545/199644
XRPX Acc No: N96-372656
Field programmable gate **array with multi-port** RAM **- has look-up table for implementing number of functions including** RAM **cells and programmable switching device for coupling and decoupling** RAM **cells**
Patent Assignee: AT & T IPM CORP (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: NGAI K; SINGH S
Number of Countries: 007 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5559450	A	19960924	US 95507957	A	19950727	199644	B
EP 756383	A2	19970129	EP 96305238	A	19960717	199710	
TW 298651	A	19970221	TW 96107452	A	19960621	199722	
JP 9083347	A	19970328	JP 96192623	A	19960723	199723	

Priority Applications (No Type Date): US 95507957 A 19950727
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5559450	A		12	H03K-019/177	
EP 756383	A2	E	12	H03K-019/177	
Designated States (Regional): DE FR GB IT					
JP 9083347	A		9	H03K-019/173	
TW 298651	A			G11C-005/06	

Abstract (Basic): US 5559450 A
The circuit includes first and second programmable elements for generating various functions including first and second respective **RAM** cells in response to a configuration bit stream, and a programmable switching device responsive to the configuration bit stream for providing bit-level coupling between the **RAM** cells so that the **RAM** cells together provide a multi-port **RAM** cell.
The programmable switching device is dedicated to coupling and decoupling the **RAM** cells which are coupled to respective first and second **read /write ports** . The **RAM** cells function individually as **single -port RAM** cells when decoupled by the switching device. However, the **RAM** cells share data to function collectively as a **dual -port RAM** cell when coupled by the switching device. The **dual - port RAM** cell is accessible by both the first and second **read / write ports** .
ADVANTAGE - Provides multi-port **RAM** with relatively little additional hardware. Exhibits highly efficient implementation of multi-port **RAM** in **FPGA** .
Dwg.1,2/6
Title Terms: FIELD; PROGRAM; GATE; ARRAY; MULTI; PORT; **RAM** ; UP; TABLE; IMPLEMENT; NUMBER; FUNCTION; **RAM** ; CELL; PROGRAM; SWITCH; DEVICE; COUPLE ; DECOUPLE; **RAM** ; CELL
Derwent Class: U13; U14; U21
International Patent Class (Main): **G11C-005/06 ; H03K-019/173 ; H03K-019/177**
International Patent Class (Additional): G11C-011/41
File Segment: EPI

19/5/13 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010019954 **Image available**
WPI Acc No: 1994-287666/199436
XRPX Acc No: N94-226546

Double port memory **switching matrix utilised as FIFO device for ATM communication network - has** single **buffered** write port **and** read port **for each** memory **of matrix with separate address and control signals**

Patent Assignee: TEXAS INSTR FRANCE (TEXI); TEXAS INSTR INC (TEXI)
Inventor: CHAUVEL G; DARRIGO S; D'ARRIGO S
Number of Countries: 011 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2702322	A1	19940909	FR 932330	A	19930301	199436	B
EP 617530	A1	19940928	EP 94400435	A	19940301	199437	
JP 7058755	A	19950303	JP 9431440	A	19940301	199518	
US 5475644	A	19951212	US 94204111	A	19940301	199604	
EP 617530	B1	20000726	EP 94400435	A	19940301	200036	
DE 69425339	E	20000831	DE 625339	A	19940301	200050	
			EP 94400435	A	19940301		

Priority Applications (No Type Date): FR 932330 A 19930301
Cited Patents: 04Jnl.Ref; EP 245996; EP 324470; EP 359551
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2702322	A1		26	H04L-012/54	
EP 617530	A1	E	18	H04L-012/56	
Designated States (Regional): CH DE ES FR GB IT LI NL SE					
JP 7058755	A		10	H04L-012/28	
US 5475644	A		9	G11C-013/00	
EP 617530	B1	E		G11C-005/02	
Designated States (Regional): CH DE ES FR GB IT LI NL SE					
DE 69425339	E			G11C-005/02	Based on patent EP 617530

Abstract (Basic): FR 2702322 A

Tn the **memory** device, each **write port** (15,23) of each **memory** has a buffered input (15) connected bit by bit by a data bus to elements of the **memory** (3,4). A column selection circuit connects to the input buffers of each row of the **memory** with lines delivering write enable signals. A decoder and write address control circuit (23), common to each row, decodes the row address and selects the line corresponding to the word in the **memory** row.

Each **reader port** (18,19) has a decoder and read address control circuit (21) which decodes a column address and selects the line corresponding to the word in the **memory** column. Read bit lines, common to each column, connect to pre-load (20), amplifier (19) and buffer (18) circuits.

USE/ADVANTAGE - In telecommunications and data processing applications. Controlling **logic circuits** occupy minimum amount of **memory** .

Dwg.5/9

Title Terms: DOUBLE; PORT; **MEMORY** ; SWITCH; MATRIX; UTILISE; FIFO; DEVICE; ATM; COMMUNICATE; NETWORK; SINGLE; BUFFER; WRITING; PORT; READ; PORT; **MEMORY** ; MATRIX; SEPARATE; ADDRESS; CONTROL; SIGNAL
Derwent Class: T01; U14; W01
International Patent Class (Main): G11C-005/02; G11C-013/00; H04L-012/28; H04L-012/54; H04L-012/56
International Patent Class (Additional): **G11C-007/00** ; H04Q-003/00; H04Q-003/52; H04Q-011/04
File Segment: EPI

22/TI/1 (Item 1 from file: 347)
DIALOG(R)File 347:(c) 2001 JPO & JAPIO. All rts. reserv.

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

22/TI/2 (Item 1 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Multiport memory **for data processor**

22/TI/3 (Item 2 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Transparent test technique for integrated circuits - has contents of context sensible registers shifted to RAM **via scan path for restoration after test session**

22/TI/4 (Item 3 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Binary to decimal number conversion apparatus - provides area which controls sequencing of microprocessor to execute decimal numeric software instructions

22/TI/5 (Item 4 from file: 350)
DIALOG(R)File 350:(c) 2001 Derwent Info Ltd. All rts. reserv.

Data processing system with separate data and memory **buses - has skew-protected register file with two read and two write input ports**

22/5/1 (Item 1 from file: 347)

03340289 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 03-003189 [JP 3003189 A]
PUBLISHED: January 09, 1991 (19910109)
INVENTOR(s): NAITO MITSUGI
SHIKATANI JUNICHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-137880 [JP 89137880]
FILED: May 31, 1989 (19890531)
INTL CLASS: [5] G11C-011/401; G01R-031/28; G11C-029/00; H01L-021/66; H01L-027/04
JAPIO CLASS: 46.1 (INSTRUMENTATION -- Measurement); 42.2 (ELECTRONICS -- Solid State Components); 45.2 (INFORMATION PROCESSING -- **Memory** Units); 46.2 (INSTRUMENTATION -- Testing
JOURNAL: Section: P, Section No. 1181, Vol. 15, No. 115, Pg. 16, March 19, 1991 (19910319)

ABSTRACT

PURPOSE: To reduce the number of external terminals for test by providing a circuit to execute the test of a **multiport memory** based on a test signal from an external part in a chip.

CONSTITUTION: By making a test mode signal TM supplied from the external part to an input terminal 4 for test into 'L', a dual port **RAM** 3 is cut off from a random **logic circuit** 2. Next, by a selecting signal PS inputted to a terminal 5, a read port is selected, and by write enable signals TWE1 and TWE2 for test inputted to terminals 8 and 9, a write port is selected. Thus, since the **multiport RAM** 3 can be considered as a **single port RAM** , the test can be executed by using a test pattern for the **single port RAM** , and the external terminals necessary for the time of inputting and outputting a test signal and test data can be reduced.

30/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013772030 **Image available**
WPI Acc No: 2001-256241/200126
XRPX Acc No: N01-182625

Programmable logic device has two sets of combinable single port memory arrays that are combined to form dual port memory arrays, are arranged in intersecting rows and columns

Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: LANE C F; MEJIA M; **REDDY S T**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6191998	B1	20010220	US 9761983	A	19971016	200126	B
			US 98107926	A	19980630		
			US 99452627	A	19991201		

Priority Applications (No Type Date): US 9761983 A 19971016; US 98107926 A 19980630; US 99452627 A 19991201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6191998	B1		21	G11C-008/00	Provisional application US 9761983 CIP of application US 98107926

Abstract (Basic): US 6191998 B1

NOVELTY - **Programmable logic** regions (88) and two sets of combinable single **port** memory arrays (84) are arranged in intersecting rows and columns. Each set of memory arrays (84) associated with other set, has rows and columns of memory cells to store data. Two sets of array (84) are combined to form dual **port** memory arrays. Interconnects (90,92) are provided to route signals between logic region and memory array.

USE - In **programmable logic device** memory arrays that consists of EPROM, EEPROM, RAM, transistors.

ADVANTAGE - Since each set of combinable single **port** memory arrays are used individually, logic resources are not wasted when dual **port** function of memory array circuit is not needed.

DESCRIPTION OF DRAWING(S) - The figure shows the **programmable logic device** .

Single **port** memory arrays (84)
Programmable logic regions (88)
Interconnects (90,92)
pp; 21 DwgNo 5/9

Title Terms: PROGRAM; LOGIC; DEVICE; TWO; SET; COMBINATION; SINGLE; **PORT** ; MEMORY; ARRAY; COMBINATION; FORM; DUAL; **PORT** ; MEMORY; ARRAY; ARRANGE; INTERSECT; ROW; COLUMN
Derwent Class: U13; U14
International Patent Class (Main): G11C-008/00
International Patent Class (Additional): G11C-007/00
File Segment: EPI

30/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013733080 **Image available**
WPI Acc No: 2001-217310/200122
Related WPI Acc No: 2000-159829; 2000-159838
XRPX Acc No: N01-154806

Integrated circuit e.g. field programmable gate array with multiport memory, transfers stored data to register so that transmitted data is accurate representation of contents of memory cells at given point of time

Patent Assignee: ALTERA CORP (ALTE-N); QUICKTURN DESIGN SYSTEMS INC (QUIC-N)
Inventor: BUTTS M R; CHEN C C; NORMAN K A; **PATEL R H** ; SAMPLE S P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6151258	A	20001121	US 97895516	A	19970716	200122	B
			US 99428019	A	19991027		

Priority Applications (No Type Date): US 97895516 A 19970716; US 99428019 A 19991027
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6151258	A		15	G11C-007/00	Div ex application US 97895516

Abstract (Basic): US 6151258 A

NOVELTY - The data stored in memory cells is transferred through a **port** into a register, so that the transmitted data is an accurate representation of the contents of memory cells at a given point of time.

USE - E.g. **field programmable gate** array (**FPGA**) with multiport memory.

ADVANTAGE - Facilitates flexible implementation of various types of logics and multiported memories in IC. Enables to change width and depth in a trade-off fashion. Enables to change width and depth of each **port** independently.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of memory cell.

pp; 15 DwgNo 4/11

Title Terms: INTEGRATE; CIRCUIT; FIELD; PROGRAM; GATE; ARRAY; MULTIPORT; MEMORY; TRANSFER; STORAGE; DATA; REGISTER; SO; TRANSMIT; DATA; ACCURACY; REPRESENT; CONTENT; MEMORY; CELL; POINT; TIME
Derwent Class: U13; U14
International Patent Class (Main): G11C-007/00
File Segment: EPI

30/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013333274 **Image available**
WPI Acc No: 2000-505213/200045
XRPX Acc No: N00-373537

Programmable logic device **has peripheral region with bidirectional peripheral input-output overflow bus that is arranged to pass control and data signals between core region and bidirectional** ports

Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: JEFFERSON D; MEJIA M; **REDDY S**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6094064	A	20000725	US 9758162	A	19970908	200045	B
			US 98121250	A	19980723		

Priority Applications (No Type Date): US 9758162 A 19970908; US 98121250 A 19980723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6094064	A		16	H03K-019/177	Provisional application US 9758162

Abstract (Basic): US 6094064 A

NOVELTY - The PLD has a core region which forms array of logic cells by interconnecting multiple logic cells with associated **programmable logic** cell conductors and a peripheral region having bidirectional **port** (260-2) selectively coupled to external circuit

and bidirectional peripheral input-output overflow bus (250) arranged to pass control and data signals between core region and bidirectional **ports** .

DETAILED DESCRIPTION - INDEPENDENT 'CLAIMS are also included for the following:

(a) method of fitting logic function in PLD;

(b) method of interconnecting bidirectional **ports** in peripheral region of PLD

USE - For coupling bidirectional **ports** .

ADVANTAGE - Enables to access logic element and memory blocks without using core region programmable connectors. By reducing the number of core region programmable connectors, complex PLD exhibits higher success rate in fitting logic functions. Since core region routing resources need not be consumed to route signals between adjacent **ports** , improved internal routability is provided.

DESCRIPTION OF DRAWING(S) - The figure shows circuit diagram of horizontal bidirectional **port** coupled to input-output overflow bus through an input-output overflow bus interface.

Input-output overflow bus (250)

Bidirectional **port** (260-2)

pp; 16 DwgNo 4/7

Title Terms: PROGRAM; LOGIC; DEVICE; PERIPHERAL; REGION; BIDIRECTIONAL; PERIPHERAL; INPUT; OUTPUT; OVERFLOW; BUS; ARRANGE; PASS; CONTROL; DATA; SIGNAL; CORE; REGION; BIDIRECTIONAL; **PORT**

Derwent Class: U21

International Patent Class (Main): H03K-019/177

File Segment: EPI

30/5/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012987985 **Image available**

WPI Acc No: 2000-159838/200014

Related WPI Acc No: 2000-159829; 2001-217310

XRPX Acc No: N00-119259

Multi- port **memory block for field** programmable logic **array**

Patent Assignee: ALTERA CORP (ALTE-N); QUICKTURN DESIGN SYSTEMS INC (QUIC-N)

Inventor: BUTTS M R; CHEN C C; NORMAN K A; **PATEL R H** ; SAMPLE S P

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6011744	A	20000104	US 97895516	A	19970716	200014	B

Priority Applications (No Type Date): US 97895516 A 19970716

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6011744	A		14	G11C-008/00	

Abstract (Basic): US 6011744 A

NOVELTY - The memory block (10) comprises a read **port** (12) that reads data out of the memory block. A write **port** (16) writes data into the memory block. The width and depth of the read **port** is independent of the write **port** .

DETAILED DESCRIPTION - The block has memory cells with configurable width and depth such that increasing the width results in decreasing the depth and decreasing the width results in increasing the depth.

USE - For a field **programmable logic** array.

ADVANTAGE - Enables implementing reconfigurable logic having a memory whose width and depth are configurable in a trade-off fashion.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the memory block.

Memory block (10)

Read **port** (12)

Write **port** (16)
pp; 14 DwgNo 1/11
Title Terms: MULTI; **PORT** ; MEMORY; BLOCK; FIELD; PROGRAM; LOGIC; ARRAY
Derwent Class: U13; U14
International Patent Class (Main): G11C-008/00
File Segment: EPI

30/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012987976 **Image available**
WPI Acc No: 2000-159829/200014
Related WPI Acc No: 2000-159838; 2001-217310
XRPX Acc No: N00-119250
Programmable logic **integrated** circuit **with integral memory block used for storing data and with** port **for taking snapshot of memory contents**
Patent Assignee: ALTERA CORP (ALTE-N); QUICKTURN DESIGN (QUIC-N)
Inventor: BUTTS M R; CHEN C C; NORMAN K A; **PATEL R H** ; SAMPLE S P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6011730	A	20000104	US 97895516	A	19970716	200014	B
			US 99298890	A	19990423		

Priority Applications (No Type Date): US 97895516 A 19970716; US 99298890 A 19990423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6011730	A		16	G11C-007/00	Cont of application US 97895516

Abstract (Basic): US 6011730 A
NOVELTY - The memory block includes a write buffer circuit which comprises a set of data inputs selectively coupled to a logic gate using selected input terminals. The output of logic is fed to another logic gate and in turn input to a different logic gate.
DETAILED DESCRIPTION - A logic element is configurable to implement user defined combinational or registered logic functions. A memory block stores data and is coupled to the logic element.
USE - For field **programmable logic** array.
ADVANTAGE - Implements reconfigurable logic whose width and depth are configurable in a tradeoff fashion. Alleviates the necessity of adding routing lines to the interconnect network.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of memory block.
pp; 16 DwgNo 3/11
Title Terms: PROGRAM; LOGIC; INTEGRATE; CIRCUIT; INTEGRAL; MEMORY; BLOCK; STORAGE; DATA; **PORT** ; SNAPSHOT; MEMORY; CONTENT
Derwent Class: U13; U14; U21
International Patent Class (Main): G11C-007/00
File Segment: EPI

30/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012425695 **Image available**
WPI Acc No: 1999-231803/199920
XRPX Acc No: N99-171756
Variable depth and width memory array for dual- port programmable logic device
Patent Assignee: ALTERA CORP (ALTE-N)
Inventor: **CLIFF R G** ; LANE C F; MEJIA M; **REDDY S T** ; VEENSTRA K
Number of Countries: 027 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 910091	A2	19990421	EP 98308159	A	19981007	199920	B
JP 11250667	A	19990917	JP 98291221	A	19981013	199949	
US 6052327	A	20000418	US 9762966	A	19971014	200026	
			US 98107533	A	19980630		

Priority Applications (No Type Date): US 98107533 A 19980630; US 9762966 A 19971014

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 910091	A2	E	20	G11C-007/00	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
US 6052327	A			G11C-008/00	Provisional application US 9762966
JP 11250667	A		21	G11C-011/41	

Abstract (Basic): EP 910091 A2

NOVELTY - Memory array has a number of rows and columns of memory cells for storing data and variable length and width writing circuitry performing write operations with selectable size data words. Reading circuitry performs read operations with selectable size data words concurrently with the write operations by addressing selected read locations within the memory array.

DETAILED DESCRIPTION - Dual **port** memory arrays (84) and **programmable logic** regions (86) are arranged in intersecting rows and columns. Each **programmable logic** region (86) may contain a number of sub-regions of **programmable logic** . Such sub-regions are based on product-term logic or look-up table logic and may include register logic for registering logic signals.

USE - In **programmable logic** systems.

ADVANTAGE - Variable depth and width data words can be written and read from array using concurrent processes.

pp; 20 DwgNo 5/10

Title Terms: VARIABLE; DEPTH; WIDTH; MEMORY; ARRAY; DUAL; **PORT** ; PROGRAM; LOGIC; DEVICE

Derwent Class: U13; U14

International Patent Class (Main): G11C-007/00; G11C-008/00; G11C-011/41

File Segment: EPI

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ile 348:EUROPEAN PATENTS 1978-2001/Jun W04
         (c) 2001 European Patent Office
File 349:PCT Fulltext 1983-2001/UB=20010621, UT=20010614
         (c) 2001 WIPO/MicroPat

Set     Items   Description
S1       5769   PROGRAMMABLE(1W)LOGIC?
S2       2034   SPLD? ? OR CPLD? ? OR FPGA? ? OR FPIC? ? OR FIELD()PROGRAM-
            MABLE()(GATE? ? OR INTERCONNECT? ? OR INTER()CONNECT? ?)
S3      32219   LOGIC?(2W)(UNIT? ? OR DEVICE? ? OR CIRCUIT?? OR MICROCIRCU-
            IT? ? OR CHIP? ? OR MODULE? ? OR BOARD? ? OR BLOCK? ? OR MICR-
            OCHIP? ? OR IC OR APPARATUS)
S4     177396   RAM OR MEMOR???
S5       4694   READ?(5N)PORT? ?
S6       2808   WRIT???(5N)PORT? ?
S7      50665   SINGLEPORT? ? OR (SINGLE OR ONE OR 1)(5N)PORT? ?
S8      54721   DUALPORT? ? OR (DUAL OR TWO OR 2 OR MULTIPLE OR MULTI OR D-
            UAL OR SEPARATE OR DIFFERENT OR TWIN OR SECOND? OR DOUBLE)(5N-
            )PORT? ? OR MULTIPORT? ?
S9       8698   IC=(H03K-007 OR H03K-019 OR G06F-007 OR G11C-007 OR G11C-0-
            08)
S10      1572   S5(S)S6
S11       172   S1 AND S10
S12        27   S11 AND S9
S13     20534   S7(S)S8
S14       472   S1 AND S13
S15        59   S14 AND S9
S16        67   S15 OR S12
S17      1015   S10(S)S4
S18      2205   S13(S)S4
S19        31   S1 AND S17:S18 AND S9
S20         7   S5(10N)S6 AND S1/TI,AB,CM AND S9
S21         1   S20 NOT S19
S22        14   S5(10N)S6(10N)S4 AND S1 AND S9
S23         0   S22 NOT S19
S24        25   S5(10N)S6 AND S1 AND S9
S25         8   S24 NOT S19
S26        44   S2:S3/TI,AB,CM AND S17:S18 AND S9
S27        28   S26 NOT (S19 OR S25)
S28         6   AU="NGAI TONY":AU="NGAI TONY ALTERA CORPORATION"
S29         5   AU="PATEL RAKESH":AU="PATEL RAKESH ALTERA CORPORATION"
S30         5   AU="REDDY SRINIVAS T"
S31        22   AU="CLIFF RICHARD":AU="CLIFF RICHARD GUY MAUD COTTAGE"
S32         4   S1:S3 AND S28:S31 AND PORT? ?
?
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19/TI/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Dual-port programmable logic device variable depth and width memory array
Programmierbare logische Vorrichtung mit zwei Anschlussen sowie Speichermatrix mit variabler Tiefe und Breite
Dispositif logique programmable; reseau de memoire a profondeur et largeur variable

19/TI/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Programmable logic array device with random access memory configurable as product terms
Programmbares logisches Feld mit als Produktterm konfigurierbarem Speicher mit wahlfreiem Zugriff
Reseau logique programmable comprenant une memoire a acces aleatoire configurable en termes de produit

19/TI/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

A synchronous semiconductor memory integrated circuit, a method for accessing said memory and a system comprising such a memory
Integrierter Schaltkreis mit synchronem Halbleiterspeicher, ein Verfahren zum Zugriff auf den besagten Speicher sowie ein System, das einen solchen Speicher bei
Circuit integre avec une memoire synchrone a semi-conducteurs, methode d'acces et systeme comprenant cette memoire

19/TI/4 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

A synchronous semiconductor memory integrated circuit, a method for accessing said memory and a system comprising such a memory
Integrierter Schaltkreis mit synchronem Halbleiterspeicher, ein Verfahren zum Zugriff auf den besagten Speicher sowie ein System, das einen solchen Speicher bei
Circuit integre avec une memoire synchrone a semi-conducteurs, methode d'acces et systeme comprenant cette memoire

19/TI/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Field programmable memory array
Benutzerprogrammierbares Speicherfeld
Reseau de memoire programmable

19/TI/6 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

A synchronous dynamic random access memory integrated circuit, a method for accessing said memory and a system comprising such a memory
Integrierte Schaltung mit synchronem Speicher mit direktem Zugriff, Methode zum Zugriff auf diesen Speicher und System mit einem solchen Speicher
Circuit integre a memoire synchrone a acces direct, methode d'acces et systeme comprenant cette memoire

19/TI/7 (Item 7 from file: 348)

DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Field programmable gate array with multi-port RAM
Benutzerprogrammierbares Gatterfeld mit Multiport-RAM
Reseau de portes programmables par l'utilisateur avec RAM multiport

19/TI/8 (Item 8 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Synchronous dual port RAM
Doppel-Torsynchroner RAM-Speicher
Memoire RAM synchrone **a** double porte

19/TI/9 (Item 9 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

A system including a synchronous DRAM
System mit einem synchronen DRAM-Speicher
Systeme avec une memoire DRAM synchrone

19/TI/10 (Item 10 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Programming a field programmable gate array and reading array status.
Programmierung einer programmierbaren Gatteranordnung und Ablesen des Zustandes einer solchen Anordnung.
Programmation d'un reseau de portes programmables et lecture de l'etat d'un tel reseau.

19/TI/11 (Item 11 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Micro-sequencer device.
Mikrofolgekontrollgerat.
Sequenceur de micro-instruction.

19/TI/12 (Item 12 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Two-wire/three-port RAM for cellular array processor.
RAM-Speicher mit zwei Linien und drei Porten fur zellularen Feldprozessor.
Memoire RAM a deux lignes et trois portes pour processeur en reseau cellulaire.

19/TI/13 (Item 13 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Cellular array processing apparatus employing multiple state logic for coupling to data buses.
Zellularer Feldprozessor mit Mehrzustandslogik zur Verbindung mit dem Datenbus.
Processeur en reseau cellulaire utilisant une logique a plusieurs etats pour le couplage vers des bus de donnees.

19/TI/14 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

INTEGRATED CIRCUIT TECHNOLOGY
TECHNIQUE RELATIVE AUX CIRCUITS INTEGRES

19/TI/15 (Item 2 from file: 349)
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FPGA INTEGRATED CIRCUIT HAVING EMBEDDED SRAM MEMORY BLOCKS AND INTERCONNECT CHANNEL FOR BROADCASTING ADDRESS AND CONTROL SIGNALS
CIRCUIT INTEGRE PREDIFFUSE PROGRAMMABLE COMPORTANT DES BLOCS MEMOIRE SRAM INCLUS ET UN CANAL D'INTERCONNEXION PERMETTANT DE DIFFUSER LES SIGNAUX D'ADRESSE ET DE COMMANDE

19/TI/16 (Item 3 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

FPGA INTEGRATED CIRCUIT HAVING EMBEDDED SRAM MEMORY BLOCKS EACH WITH STATICALLY AND DYNAMICALLY CONTROLLABLE READ MODE
CIRCUIT INTEGRE DE TYPE PREDIFFUSE PROGRAMMABLE (FPGA) A BLOCS MEMOIRES SRAM INCLUS CAPABLES CHACUN D'UN MODE DE LECTURE A COMMANDE STATIQUE ET DYNAMIQUE

19/TI/17 (Item 4 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

EMBEDDED STATIC RANDOM ACCESS MEMORY FOR FIELD PROGRAMMABLE GATE ARRAY
MEMOIRE VIVE STATIQUE ENFOUIE, DESTINEE A UN RESEAU DE PORTES PROGRAMMABLE

19/TI/18 (Item 5 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

DATA ROUTING DEVICES
DISPOSITIFS D'ACHEMINEMENT DE DONNEES

19/TI/19 (Item 6 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

MEMORY INCLUDING RESISTOR BIT;ndash;LINE LOADS
MEMOIRE COMPRENANT DES CHARGES DE LIGNES DE BINAIRE RESISTIVES

19/TI/20 (Item 7 from file: 349)
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METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE
PROCEDE ET APPAREIL DESTINES A UNE ARCHITECTURE DE BUS COMMANDE PAR UN PROGRAMME UNIVERSEL

19/TI/21 (Item 8 from file: 349)
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FPGA ARCHITECTURE HAVING RAM BLOCKS WITH PROGRAMMABLE WORD LENGTH AND WIDTH AND DEDICATED ADDRESS AND DATA LINES
ARCHITECTURE FPGA A BLOCS DE MEMOIRE RAM POUR LONGUEUR ET LARGEUR DE MOT PROGRAMMABLES ET POUR LIGNES D'ADRESSES ET DE DONNEES SPECIALISEES

19/TI/22 (Item 9 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

METHOD AND SYSTEM FOR PERFORMING A CORRELATION OPERATION
PROCEDE ET SYSTEME PERMETTANT UNE OPERATION DE CORRELATION

19/TI/23 (Item 10 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

METHOD AND SYSTEM FOR PERFORMING AN L1 NORM OPERATION
PROCEDE ET DISPOSITIF PERMETTANT DE REALISER UNE OPERATION EN NORME L1

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METHOD AND SYSTEM FOR PERFORMING AN L2 NORM OPERATION
PROCEDE ET DISPOSITIF CONCERNANT UNE OPERATION EN NORME L2

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METHOD AND SYSTEM FOR PERFORMING AN IIR FILTERING OPERATION
PROCEDE ET SYSTEME DESTINES A L'EXECUTION D'UNE OPERATION DE FILTRAGE A REPONSE IMPULSIONNELLE INFINIE

19/TI/26 (Item 13 from file: 349)
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COMPUTER PROCESSOR HAVING A PIPELINED ARCHITECTURE AND METHOD OF USING SAME
PROCESSEUR D'ORDINATEUR AYANT UNE ARCHITECTURE EN PIPELINE ET PROCEDE D'UTILISATION DUDIT PROCESSEUR

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DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

COMPUTER PROCESSOR HAVING A PIPELINED ARCHITECTURE WHICH UTILIZES FEEDBACK AND METHOD OF USING SAME
PROCESSEUR D'ORDINATEUR AYANT UNE STRUCTURE PIPELINE ET A RETROACTION, ET PROCEDE D'UTILISATION

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DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

METHOD AND SYSTEM FOR PERFORMING AN FIR FILTERING OPERATION
PROCEDE ET DISPOSITIF DE FILTRAGE A REPONSE IMPULSIONNELLE FINIE

19/TI/29 (Item 16 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

APPARATUS FOR PROGRAMMABLE CIRCUIT AND SIGNAL SWITCHING
DISPOSITIF DESTINE A UN CIRCUIT PROGRAMMABLE ET A LA COMMUTATION DE SIGNAUX

19/TI/30 (Item 17 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

A STRUCTURED PROGRAMMABLE DATAPATH FOR A DIGITAL PROCESSOR
CHEMIN DE DONNEES PROGRAMMABLE STRUCTURE POUR PROCESSEUR NUMERIQUE

19/TI/31 (Item 18 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

A FIELD PROGRAMMABLE GATE ARRAY
RESEAU DE PORTES PROGRAMMABLE PAR L'UTILISATEUR

19/5/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00814285

Field programmable gate array with multi-port RAM
Benutzerprogrammierbares Gatterfeld mit Multiport-RAM
Reseau de portes programmables par l'utilisateur avec RAM multiport

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DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: **H03K-019/177**

ABSTRACT EP 756383 A2

A field programmable gate array (FPGA) with a programmable function unit (PFU) that includes a look-up table (LUT) for implementing a plurality of functions including first and second **RAM** cells (102, 108), and a programmable switching device (114) dedicated to coupling and decoupling the **RAM** cells. The first and second **RAM** cells are coupled to respective first and **second read /write ports** (104, 110). The **RAM** cells function individually as **single -port RAM** cells when decoupled by the switching device. However, the **RAM** cells share data to function collectively as a **dual -port RAM** cell when coupled by the switching device. The **dual -port RAM** cell is accessible by both the first and **second read /write ports** .

ABSTRACT WORD COUNT: 113

19/5/5 (Item 5 from file: 348)
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00844714
Field programmable memory array
Benutzerprogrammierbares Speicherfeld
Reseau de memoire programmable
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ABSTRACT EP 780846 A2
A field programmable memory array having a plurality of sub-arrays is provided. Programmable address decoders, programmable hierarchical bit line arrangements, programmable I/O arrangements, among other features, are provided to enable programming of portions of the array into selected modes. The modes may include wide memory, deep memory, FIFO, LIFO, among others. An embodiment of the invention is disclosed wherein the field programmable memory array is integrated with the programmable resources of a field programmable gate array.
ABSTRACT WORD COUNT: 77

Description

This invention relates to data memory and more specifically to a programmable memory array with associated programmable routing and control resources. This invention also relates to a programmable memory array incorporated together with a field programmable gate array.

Known integrated memory arrays generally have a fixed depth and fixed width as associated with a given data storage application. Accordingly, different data storage applications may require separate respective memory arrays for meeting the different depth/width requirements. However, it would be advantageous if a single memory resource were capable of meeting the different depth/width application needs.

A variety of known memory devices are available for providing different memory access techniques. The most common memory access technique includes simple addressable read/write memory functionality. Other access techniques include LIFO (Last In First Out), FIFO (First In First Out) and rollover data stack operations. Existing data storage devices are generally tailored to specific, fixed access techniques. However, it would be advantageous if a memory device were programmable to selectively provide combinations of access techniques.

Programmable integrated circuits are known in the art and include programmable gate arrays (PGA) which provide an array of distinct, uncommitted logic cells. A programmable interconnect network is usually provided for interconnecting the cells and/or to provide data input to and output from the array. Customization or programming of the otherwise generally designed logic cells and interconnect network is performed for implementing a particular application. One such device is a field-programmable gate array (FPGA), wherein the configuration of the FPGA can be performed by a user "in the field." The configuration of the FPGA is effected by using electrically programmable fusible links, antifuses, memory controlled transistors or floating gate transistors. To program the FPGA, configuration data is transferred from an external memory device to electrically programmable resources of the FPGA. As densities of these field programmable gate arrays increase, the demand for on-board memory/storage functionality likewise increases. Accordingly, it would be desirable to provide an integrated circuit including an FPGA together with a programmable memory array, which memory array could be capable of implementing various configurations, and/or provide one of a variety of memory access techniques.

Accordingly, it is an object of at least an embodiment of the present invention to provide an improved memory array.

It is a another such object to provide a programmable memory array that is programmably configurable for providing a variety of data storage architectures.

It is a further such object to provide a memory array selectively programmable for implementing a variety of memory access techniques.

It is yet a further such object to provide an integrated circuit incorporating a field programmable gate array together with a programmable memory array.

It is yet a further such object to provide an integrated circuit incorporating a field programmable gate array together with a field programmable memory array, wherein the field programmable memory array is accessible during configuration of the field programmable gate array, during reconfiguration of the field programmable gate array, or during normal functionality of the field programmable gate array.

In one aspect of the invention there is provided a programmable memory array having multiple sub-arrays of memory cells therein and support circuitry including input/output circuitry, address lines, data lines and decode circuitry, the programmable memory array comprising:

configuration circuitry connected within the support circuitry and having user-programmable elements therein for configuring the support circuitry to provide a respective user-selected access mode for each of the multiple sub-arrays of the array, the multiple sub-arrays being operable simultaneously in their respective user-selected modes.

The embodiment of the present invention is, in one aspect, a field programmable memory array having a plurality of memory sub-arrays. The memory sub-arrays are selectively programmable for implementing a variety of different memory configurations and operating modes. In general, each sub-array can be programmed into, and thereafter accessed using, one of a set of modes. The set of modes includes, in one embodiment, wide RAM, deep RAM, FIFO and LIFO.

Numerous programmable structures are provided to effect the programming of the portions of the memory array. For example, the array may include an address decoder and a programmable access unit for providing read and write input addresses to the address decoder during associated read and write operations of the memory array. The programmable access unit may further comprise a first address counter, a first clock control unit and an address comparison unit.

The bit lines of the memory array are placed into a programmable, hierarchical arrangement. Local bit lines, semi-global bit lines and global bit lines can be provided and are programmably interconnectable to provide a high degree of bit line programmability. Further, the interconnected bit line structure is programmably connectable to I/O buses.

A primary I/O bus and a secondary I/O bus can be provided, along with first and second selective couplers for programmable connections thereto.

A programmable address decoder may be provided having M word lines, a plurality of address lines propagating address data, and a decoder circuit for selectively driving a given word line of the M word lines as selected in accordance with address data of the plurality of address lines. A selective coupler can also be provided having a plurality of inputs coupled to an associated set of lines of an address bus, and an output coupled to an address line of the plurality of address lines, the selective coupler selectively coupling its output to one of its plurality of inputs in accordance with programming data.

A selective read capture latch can be provided for selectively interfacing to the hierarchical bit line structure. The selective read capture latch may include at least first and second hierarchy inputs, a memory unit having an input and an output, and selective coupling means between the first and second hierarchy inputs and the input of the memory unit, for selectively coupling one of the first and second hierarchy inputs to the input of the memory unit for propagating data therebetween in accordance with an associated hierarchy read capture clock. Precharge means may be provided for pre-charging at least one bit line of the hierarchical bit line structure.

In alternate embodiments, programmable transfer paths and scan chain latches can be provided between the memory cells of the array to provide a physical LIFO/FIFO function, as well as provide testability for the cells and related paths in the array, respectively.

In a preferred embodiment, the field programmable memory array (FPMA) disclosed herein can be integrated with the programmable logic cells of a field programmable gate array (FPGA) to provide a fully programmable logic system which includes highly programmable combinational and memory circuitry.

The aforementioned, along with numerous other features of the present invention, disclosed below, provide a significant improvement over prior art memory systems wherein the memory access technique was fixed, offering little or no flexibility for user access thereto.

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of practice, together with further objects and advantages thereof, may best be understood by reference to the following detailed description of the preferred embodiments and the accompanying drawings in which:

Figs. 1A-1E depict, at various levels, a field programmable memory array of the present invention;
Figs. 2A-2B provide a partial schematic diagram of a memory sub-array;
Fig. 3 is a schematic diagram of a memory cell;
Fig. 4 is a schematic diagram of an alternative memory cell;
Fig. 5 is a schematic diagram of a transfer cell;
Figs. 6A-6E are partial schematic diagrams of a bit line routing matrix;
Fig. 7 is a schematic diagram of a switching matrix element associated with the bit line routing matrix of **Fig. 6A** and a read bit line hierarchy structure;
Fig. 8 is a schematic diagram of a switching matrix element associated with the bit line routing matrix of **Fig. 6B** and a write bit line hierarchy structure;
Fig. 9 is a schematic diagram of a switching matrix element associated with the bit line routing matrix of **Fig. 6C** and a push bit line;
Fig. 10 is a schematic diagram of a switching matrix element associated with the bit line routing matrix of **Fig. 6D** and a pop bit line;
Fig. 11 is a block diagram of an I/O routing matrix;
Fig. 12 is a partial schematic diagram of a write matrix switch of the I/O routing matrix of **Fig. 11**;
Fig. 13 is a partial schematic diagram of a read matrix switch of the I/O routing matrix of **Fig. 11**;
Fig. 14 is a block diagram of an I/O block;
Fig. 15 is a schematic diagram of an I/O cell of the I/O block of **Fig. 14**;
Fig. 16 is a partial schematic diagram of an alternative read/write bit line hierarchy structure;
Fig. 17 is a partial schematic diagram illustrating a higher order alternative read/write bit line hierarchy structure;
Figs. 18A-18B are partial schematic diagrams of a read data path network incorporating the alternative read bit line hierarchy structure associated with four memory sub-arrays;
Fig. 19 is a partial schematic diagram of a write port data path network incorporating the alternative write bit line hierarchy structure associated with four memory sub-arrays;
Fig. 20 is a simplified schematic diagram of a read bit line hierarchy structure incorporating alternative read capture latch banks;
Fig. 21 is a block diagram of a capture latch bank as shown in **Fig. 20**;
Fig. 22 is a schematic diagram of a clock generator of **Fig. 21**;
Fig. 23 is a schematic diagram showing a single cell of a read capture latch bank of **Fig. 21**;
Fig. 24 is a schematic diagram of a precharge circuit;
Fig. 25 is a schematic diagram showing precharge circuitry incorporated within a read capture latch;

at least one sub-array having a plurality of memory cells;
a line for propagating memory cell data away from the cells of the at least one sub-array;
a precharge device programmably connectable to the line; and
a drive device connected between the cells of the at least one sub-array and the line, the drive device programmably operable in a first mode wherein discharge of the said line in accordance with the memory cell data is effected, and a second mode wherein drive of said line in accordance with the memory cell data is effected.

165. The programmable memory array of clause 164, wherein the precharge device is connected to the line in the first mode and disconnected from the line in the second mode.

166. The programmable memory array of clause 165, wherein the first mode comprises synchronous sub-array operation and the second mode compromises asynchronous sub-array operation.

167. The programmable memory array of clause 164, wherein the drive device is programmably operable in a third mode wherein a high impedance is provided to the line.

Claims

1. A programmable memory array having multiple sub-arrays of memory cells therein and support circuitry including input/output circuitry, address lines, data lines and decode circuitry, the programmable memory array comprising:
configuration circuitry connected within the support circuitry and having user-programmable elements therein for configuring the support circuitry to provide a respective user-selected access mode for each of the multiple sub-arrays of the array, the multiple sub-arrays being operable simultaneously in their respective user-selected modes.

2. The programmable memory array of claim 1, further comprising a configuration memory connected to the configuration circuitry for holding user-selected access mode information.

3. The programmable memory array of claims 1 or 2, wherein each respective user-selected access mode can be selected from the group consisting of wide memory and deep memory.

4. The programmable memory array of claims 1 or 2, wherein each respective user-selected access mode can be selected from the group consisting of FIFO, wide memory and deep memory.

5. The programmable memory array of claims 1 or 2, wherein each respective user-selected access mode can be selected from the group consisting of single port memory and dual port memory.

6. The programmable memory array of claims 1 or 2, wherein each respective user-selected access mode can be selected from the group consisting of single port and dual port register arrays.

7. A programmable gate array having a plurality of programmable logic cells therein, the programmable gate array further comprising a programmable memory array as set forth in any one of the preceding claims.

8. The programmable memory array of any one of claims 1 to 6 wherein a respective user-selected access mode comprises a read-only memory.

9. A programmable memory array, comprising:

at least one sub-array having a plurality of memory cells;

a line for propagating memory cell data away from the cells of the at least one sub-array;

a precharge device programmably connectable to the line; and

a drive device connected between the cells of the at least one sub-array and the line, the drive device programmably operable in a first mode wherein discharge of the said line in accordance with the memory cell

data is effected, and a second mode wherein drive of said line in accordance with the memory cell data is effected.

10. A programmable memory circuit comprising:

a memory cell for holding data;

a first word line that propagates a first select signal;

a first bit line;

a first selective coupler disposed between said first bit line and said memory cell, selectively coupling said first bit line and said memory cell in accordance with said first select signal for propagating a signal therebetween;

an output interface connected to said memory cell for carrying a signal from said memory cell; and

an additional data line connected to said memory cell for carrying a signal to said memory cell.

11. A programmable memory circuit comprising:

a memory cell for holding data;

a plurality of word lines, each word line of said plurality of word lines propagating an associated enable signal;

a plurality of bit lines; and

a plurality of selective couplers, each selective coupler of said plurality of selective couplers being disposed between said memory cell and an associated bit line of said plurality of bit lines, selectively coupling said associated bit line and said memory cell for propagating a signal therebetween when enabled by the enable signal of an associated word line of said plurality of word lines.

12. A programmable memory circuit comprising an array of bit/word line addressable memory cells including:

a first memory cell addressable per a first word line for enabling primary data access thereto;

a second memory cell addressable per a second word line, for enabling primary data access thereto;

a transfer cell disposed intermediate said first memory cell and said second memory cell for providing intermediate data storage;

a first selective coupler enabled per a first clock for selectively coupling said transfer cell and said first memory cell, enabling data propagation therebetween; and

a second selective coupler enabled per a second clock for selectively coupling said transfer cell and said second memory cell, enabling data propagation therebetween;

whereby said first and second clocks are operated sequentially for transferring data from one of said first and second memory cells to the other.

13. A method of operating a FPGA and a programmable memory array, said method including the steps of:

configuring the FPGA, including transferring initial data from an external data source into said programmable memory array; and

functionally operating said configured FPGA, including internally accessing said programmable memory array.

14. A memory array comprising a plurality of memory cells arranged in rows and columns, each row of memory cells

having associated therewith an addressable enable word line, and each column of memory cells having associated therewith a bit line, each bit line providing access to memory cells of said associated column as enabled via respective addressable enable word lines, said memory array further comprising:

a plurality of discrete couplers, each discrete coupler of the plurality of discrete couplers being disposed between respective adjacent memory cells of a given column;

each discrete coupler being operative for selectively shifting data within the given column from one of the respective adjacent memory cells to the other in accordance with a push/pop control signal.

15. A memory array comprising a plurality of memory cells arranged in rows and columns, each row of cells having associated therewith a word line selectively addressable by an associated row address, and each column of cells having associated therewith a bit line that provides access to memory cells of said associated column as enabled via respective word lines, said memory array further comprising:

an address decoder having an address input for receiving an input address, said address decoder selecting said word lines in accordance with said input address; and

a programmable access unit for providing read and write input addresses to the address input of said address decoder during associated read and write operations of said memory array, said programmable access unit modifying said read and write addresses during operations of said memory array so as to provide one of Last In First Out (LIFO), or First In First Out (FIFO), memory functionality in accordance with a mode select signal.

16. A programmable memory array having a plurality of memory cells arranged in rows and columns, a row of cells having an associated word line, and a column of cells having associated therewith a programmable bit line structure, said programmable bit line structure of the column of cells comprising:

a plurality of local bit lines, each local bit line of said plurality of local lines being associated with a respective sub-array group of memory cells of said given column of cells; and

a local selective coupler between adjacent local bit lines of said plurality of local bit lines, said selective coupler being programmable for selectively propagating a signal therebetween.

17. A programmable intercoupling circuit of a programmable memory array having a primary I/O bus and a secondary I/O bus, said programmable intercoupling circuit comprising:

a first selective coupler having an output and a plurality of inputs, inputs of said plurality of inputs being coupled to select primary interconnects of said primary I/O bus interconnects, said first selective coupler being programmable for selectively propagating a signal between said output and one input of said plurality of inputs in accordance with a first select signal; and

a second selective coupler having an input electrically coupled for receiving a signal associated with the output of said first selective coupler, and a plurality of outputs, outputs of said plurality of outputs being coupled to select secondary interconnects of said secondary I/O bus, said second selective coupler being programmable for selectively propagating a signal between said input and one output of said plurality of outputs in accordance with a second select signal.

18. A programmable intercoupling circuit of a programmable memory array having a primary I/O bus and a secondary I/O bus, said programmable intercoupling circuit comprising:

a programmable read port having means for selectively propagating, in accordance with a first select signal, a first signal from a select secondary interconnect of said secondary I/O bus to a select primary interconnect of said primary I/O bus; and

a programmable write port having means for selectively propagating, in accordance with a second select signal, a second signal from a select primary interconnect of said primary I/O bus to a select secondary interconnect of said secondary I/O bus.

19. A programmable address decoder comprising:

M word lines;

a plurality of address lines for propagating address data;

a programmable inverter disposed in series with a given address line of said plurality of address lines, said programmable inverter selectively inverting a signal propagating along said given address line in accordance with an address polarity select signal; and

a decoder circuit selectively driving a given word line of said M word lines as selected in accordance with address data of said plurality of address lines as processed per said programmable inverter.

20. A programmable address decoder comprising:

M word lines;

a plurality of address lines for propagating address data;

a decoder circuit selectively driving a given word line of said M word lines as selected in accordance with address data of said plurality of address lines; and

a selective coupler having a plurality of inputs coupled to an associated set of lines of an address bus, and an output coupled to an address line of said plurality of address lines, said selective coupler selectively coupling its output to one of its plurality of inputs in accordance with associated configuration data.

21. A programmable address decoder comprising:

M word lines;

a plurality of address inputs for receiving address data;

an enable input for receiving an enable signal;

logic means for selectively driving one word line of said M word lines when its associated address data is received at said plurality of address inputs and when enabled per said enable signal; and

programmable means for providing said enable signal in accordance with an enable select signal.

22. A memory array having:

a plurality of memory cells arranged in rows and columns, said rows of memory cells being selectable per respective word lines for loading data therein, said plurality of memory cells sharing a common reset signal; and

a programmable address decoder having M word line outputs coupled to the respective word lines of said plurality of rows of memory cells, a plurality of inputs for receiving address data for addressing select word line outputs in accordance with said address data, and a reset disable input for receiving said common reset signal, said programmable address decoder disabling said M word line outputs in accordance with said common reset signal.

23. A programmable memory array comprising:

a plurality of memory sub-arrays, each memory sub-array including a plurality of memory cells arranged in rows and columns, a plurality of local bit lines wherein each column of memory cells has an associated local bit line of said plurality of local bit lines for presenting/receiving data to/from the memory cells thereof, and a plurality of word lines wherein each row of said plurality of memory cells has an associated word line providing a select signal for controlling access of the memory cells of said row to associated local bit lines; and

a programmable bus matrix for selectively configuring local bit lines of the various memory sub-arrays;

said programmable bus matrix being programmable in a first configuration wherein the local bit lines of one sub-array of said plurality of sub-arrays are electrically intercoupled to corresponding local bit lines of another sub-array of said plurality of sub-arrays so as to provide common bit lines for the respective memory cells of the corresponding columns of said one and said another sub-arrays; and

said programmable bus matrix being programmable in a second configuration wherein the local bit lines of said one sub-array of said plurality of sub-arrays are electrically configured in parallel with corresponding local bit lines of said another sub-array of said plurality of sub-arrays so as to provide separate, parallel bit lines for accessing the memory cells of the corresponding columns of said one and said another sub-arrays.

24. A memory array comprising:

Z memory blocks, each of said memory blocks comprising a generally rectangular sub-array of M x N memory cells;

address lines connectable to each of said memory blocks;

data lines connectable to each of said memory blocks;

I/O circuitry; and

programming elements distributed within said address lines, data lines, and I/O circuitry such that at least one portion of said Z memory blocks can be configured into an iM x jN memory, wherein i and j are positive integers, by programming said programming elements.

25. A bit line hierarchy structure for a plurality of memory units, comprising:

a plurality of first hierarchy bit lines, each first hierarchy bit line being associated with a given memory unit of the plurality of memory units;

a plurality of second hierarchy bit lines, each second hierarchy bit line being associated with a different respective grouping of memory units of the plurality of memory units, each second hierarchy bit line partially overlapping at least one other second hierarchy bit line wherein the respective groupings of memory units of said each second hierarchy bit line and said one other second hierarchy bit line share a common memory unit; and

selective multiplexer means provided with each memory unit for selectively coupling said each memory unit to one of its associated first and second hierarchy bit lines.

26. A selective read capture latch for selectively interfacing a hierarchal bit line structure, said selective read capture latch comprising:

at least first and second hierarchy inputs for receiving data from respective first and second hierarchy bit lines of the hierarchical bit line structure;

a memory unit having an input and output, said memory unit for retaining data per data received at its input, and providing output data at its output per data retained therein; and

selective coupling means between said at least first and second hierarchy inputs and said input of said memory unit, for selectively coupling one of said first and second hierarchy inputs to said input of said memory unit for propagating data therebetween in accordance with an associated hierarchy read capture clock.

27. A programmable memory array having a plurality of memory cells arranged in rows and columns, each row of cells having an associated addressable word line, and each column of cells having associated therewith a programmable bit line structure, said programmable bit line structure comprising:

a plurality of first hierarchy bit lines, each of at least two first hierarchy bit lines of said plurality of first hierarchy bit lines being associated with a respective sub-array group of memory cells of said given column of cells;

a second hierarchy bit line associated with a respective segment of memory cells of said given column, said segment encompassing said sub-array groups of memory cells of said given column as associated with said at least two first hierarchy bit lines;

an internal sub-array bit line associated with each sub-array group of memory cells, said internal sub-array bit lines providing propagation of data as read from a given memory cell of its associated sub-array group in said given column as addressably enabled per its associated row word line;

a selective coupler for at least one of said programmable internal sub-array bit lines, in accordance with given hierarchical configuration data for selectively propagating a signal between its associated internal sub-array bit line and one bit line of the group including at least one of said first hierarchy bit lines said second hierarchy bit lines;

a read port for outputting data as read from the given memory cell of said given column of memory cells; and

a selective read capture latch for selectively capturing data therein from a select bit line of at least one of said first hierarchy bit lines and said second hierarchy bit line, and having an output for providing said captured data to said read port.

27/TI/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Delay line for recirculating ALU output data to its input
Verzogerungsleitung zum Ruckfuhren von ALE-Ausgangsdaten zu deren Eingang
Ligne de retard pour reboucler des donnees de sortie d'une UAL a son entree

27/TI/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Memory system and data communications system
Speichersystem und Datenkommunikationssystem
Systeme de memoire et systeme de communications de donnees

27/TI/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Video compression/decompression using discrete cosine transformation.
Video-Kompression und Dekompression mit Anwendung der diskreten Cosinustransformation.
Compression et decompression de signaux video utilisant la transformee discrete du cosinus.

27/TI/4 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Integrated circuit memory device with redundant rows
Integrierte Speicherschaltung mit redundanten Zeilen
Dispositif de memoire avec circuit integre ayant des lignes redondantes

27/TI/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Control circuit for dual port memory
Steuerschaltung fur Zwei-Torspeicher
Circuit de commande pour memoire a double porte

27/TI/6 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Control circuit for dual port memory
Steuerschaltung fur Zwei-Tor-Speicher
Circuit de commande pour memoire a double porte

27/TI/7 (Item 7 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Arithmetic circuit, and adaptive filter and echo canceler using it.
Arithmetische Schaltung fur adaptive Filter und Echoausloscher.
Circuit arithmetique pour filtre adaptif et dispositif d'extinction d'echo.

27/TI/8 (Item 8 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Multi-port static random access memory with fast write-thru scheme
Multiport statischer Direktzugriffspeicher mit schnellem Schreibdurchschema
Memoire statique multiporte a acces aleatoire avec scheme d'ecriture a travers

27/TI/9 (Item 9 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Multiport RAM and information processing unit
Multitor-RAM und Datenverarbeitungseinheit
RAM multiport et unite de traitement d'information

27/TI/10 (Item 10 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Memory organization with arrays having an alternate data port facility.
Speicheranordnung mit Felder und der Moglichkeit von sich abwechselnden Datentoren.
Organisation de memoire avec des reseaux ayant la faculte de portes de donnees alternees.

27/TI/11 (Item 11 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Single-fifo high speed combining switch.
Hochgeschwindigkeits-Kombinierschalter mit Einzelfifo.
Commutateur de combinaison a grande vitesse utilisant un seul tampon PEPS.

27/TI/12 (Item 12 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Semiconductor integrated circuit device and system using the same
Integrierte Halbleiterschaltung und System unter Verwendung derselben Schaltung
Circuit integre a semi-conducteurs et systeme utilisant le meme circuit

27/TI/13 (Item 13 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Data buffer apparatus and method.
Datenpuffervorrichtung und -verfahren.
Methode et systeme tampon de donnees.

27/TI/14 (Item 14 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Digital signal processor.
Digitaler Signalprozessor.
Processeur de traitement numerique de signaux.

27/TI/15 (Item 15 from file: 348)
DIALOG(R)File 348:(c) 2001 European Patent Office. All rts. reserv.

Sequential logic circuit.
Sequentielle logische Schaltung.
Circuit logique sequentiel.

27/TI/16 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

ELECTRIC/ELECTRONIC CIRCUIT DEVICE
DISPOSITIF A CIRCUIT ELECTRIQUE/ELECTRONIQUE

27/TI/17 (Item 2 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

METHOD FOR MULTIPLICATION IN GALOIS FIELDS USING PROGRAMMABLE CIRCUITS
PROCEDE DE MULTIPLICATION EN CHAMPS DE GALOIS A L'AIDE DE CIRCUITS PROGRAMMABLES

27/TI/18 (Item 3 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

PARALLEL DATA PROCESSING APPARATUS
APPAREIL DE TRAITEMENT DE DONNEES PARALLELE

27/TI/19 (Item 4 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

DEVICE CONTAINING A MULTI-PORT MEMORY
DISPOSITIF CONTENANT UNE MEMOIRE MULTI-PORT

27/TI/20 (Item 5 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

A LOW LATENCY DRAM CELL AND METHOD THEREFOR
CELLULE DE MEMOIRE RAM DYNAMIQUE ET PROCEDE ASSOCIE

27/TI/21 (Item 6 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING BY TIME MULTIPLEXING A DECODE PATH
MEMOIRE REMANENTE PERMETTANT DES OPERATIONS DE LECTURE ET D'ECRITURE SIMULTANEES PAR MULTIPLEXAGE TEMPOREL D'UNE VOIE DE DECODAGE

27/TI/22 (Item 7 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

MULTIPLE PARALLEL IDENTICAL FINITE STATE MACHINES WHICH SHARE COMBINATORIAL LOGIC
MULTIPLES MACHINES A ETATS FINIS IDENTIQUES PARALLELES QUI PARTAGENT UNE LOGIQUE COMBINATOIRE

27/TI/23 (Item 8 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

SYSTEM FOR PERFORMING ARITHMETIC OPERATIONS WITH SINGLE OR DOUBLE PRECISION
SYSTEME POUR EFFECTUER DES OPERATIONS ARITHMETIQUES EN MODE PRECISION SIMPLE OU DOUBLE

27/TI/24 (Item 9 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

SEMICONDUCTOR MEMORY DEVICE FOR BLOCK ACCESS APPLICATIONS
MEMOIRE A SEMI-CONDUCTEUR POUR APPLICATIONS D'ACCES PAR BLOC

27/TI/25 (Item 10 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

MULTI-PORT MEMORY DEVICE WITH MULTIPLE SETS OF COLUMNS
DISPOSITIF DE MEMOIRE MULTI-PORT A ENSEMBLES DE COLONNES MULTIPLES

27/TI/26 (Item 11 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

VIDEO COMPRESSION/DECOMPRESSION PROCESSING AND PROCESSORS
PROCEDE ET PROCESSEURS DE COMPRESSION/DECOMPRESSION VIDEO

27/TI/27 (Item 12 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

METHOD AND APPARATUS FOR A SPECIAL PURPOSE ARITHMETIC BOOLEAN UNIT
PROCEDE ET APPAREIL POUR UNE UNITE BOOLEENNE ARITHMETIQUE SPECIALISEE

27/TI/28 (Item 13 from file: 349)
DIALOG(R)File 349:(c) 2001 WIPO/MicroPat. All rts. reserv.

APPARATUS FOR PIPELINING A STORAGE SYSTEM
APPAREIL PERMETTANT DE COMMUNIQUER AVEC UN SYSTEME DE MEMORISATION
?

32/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01015192
Dual- port programmable logic device **variable depth and width memory array**
Programmierbare logische Vorrichtung mit zwei Anschlussen sowie Speichermatrix mit variabler Tiefe und Breite
Dispositif logique programmable; reseau de memoire a profondeur et largeur variable
PATENT ASSIGNEE:
Altera Corporation, (398574), 101 Innovation Drive, San Jose, California 95134, (US), (Applicant designated States: all)
INVENTOR:
Reddy, Srinivas T. , Altera Corporation, 101 Innovation Drive, San Jose, California 95134, (US)
Lane, Christopher F., Altera Corporation, 101 Innovation Drive, San Jose, California 95134, (US)
Mejia, Manuel, Altera Corporation, 101 Innovation Drive, San Jose, California 95134, (US)
Cliff, Richard G. , Altera Corporation, 101 Innovation Drive, San Jose, California 95134, (US)
Veenstra, Kerry, Altera Corporation, 101 Innovation Drive, San Jose, California 95134, (US
LEGAL REPRESENTATIVE:
Hogg, Jeffery Keith et al (31905), Withers & Rogers, Goldings House, 2 Hays Lane, London SE1 2HW, (GB)
PATENT (CC, No, Kind, Date): EP 910091 A2 990421 (Basic)
EP 910091 A3 991027
APPLICATION (CC, No, Date): EP 98308159 981007;
PRIORITY (CC, No, Date): US 62966 P 971014; US 107533 980630
DESIGNATED STATES: DE; FR; GB; IT; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G11C-007/00; H03K-019/177

ABSTRACT EP 910091 A2
A dual-**port programmable logic device** memory array is provided. Selectable-size data words may be written to and read from the array concurrently. Data is written into the array using write column decoder and data selection logic. The size of the data words handled by the write column decoder and data selection logic is controlled by mode select signals. Data is read from the array using read column decoder and data selection logic. The size of the data words handled by the read column decoder and data selection logic is also controlled by mode select signals. The write column decoder and data selection logic may be used to write data into the memory array at one selected location at the same time that the read column decoder and data selection logic is used to read data from the array at another selected location. A write row address decoder and a read row address decoder are used to independently address individual rows of memory cells in the memory array during writing and reading, respectively.
ABSTRACT WORD COUNT: 173
NOTE:
Figure number on first page: 5

LEGAL STATUS (Type, Pub Date, Kind, Text):
Examination: 20000322 A2 Date of request for examination: 20000121
Application: 990421 A2 Published application (A1with Search Report ;A2without Search Report)
Change: 991027 A2 International Patent Classification changed: 19990909
Search Report: 991027 A3 Separate publication of the search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count

CLAIMS A	(English)	9916	1176
SPEC A	(English)	9916	6931
Total word count - document A			8107
Total word count - document B			0
Total word count - documents A + B			8107

32/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00804264
Interconnection architecture for coarse-grained programmable logic device
Verbindungsarchitektur fur programmierbare logische Vorrichtung mit grobkorniger Oberflachenstruktur
Architecture d'interconnexion pour reseaux logique/programmable a granulation grossiere
PATENT ASSIGNEE:
ALTERA CORPORATION, (398573), 2610 Orchard Parkway, San Jose, California 95035, (US), (applicant designated states: DE;FR;GB;IE;NL)
INVENTOR:
Cliff, Richard G. , 194 Smithwood Street, Milpitas, California 95035, (US
LEGAL REPRESENTATIVE:
Cross, Rupert Edward Blount et al (42891), BOULT WADE TENNANT 27 Furnival Street, London EC4A 1PQ, (GB)
PATENT (CC, No, Kind, Date): EP 748049 A2 961211 (Basic)
EP 748049 A3 971119
APPLICATION (CC, No, Date): EP 96303978 960531;
PRIORITY (CC, No, Date): US 484831 950607
DESIGNATED STATES: DE; FR; GB; IE; NL
INTERNATIONAL PATENT CLASS: H03K-019/177;

ABSTRACT EP 748049 A2
A new **programmable logic device** architecture with an improved LAB and improved interconnection resources. For interconnecting signals to and from the LABs (200), the global interconnection resources include switch boxes (310), long lines (340 and 350), double lines (360 and 370), single lines (385), and half- (330) and partially populated (320) multiplexer regions. The LAB includes two levels of function blocks. In a first level, there are eight four-input function blocks (601). In a second level, there are two four-input function blocks (670) and four secondary two-input function blocks (672). In one embodiment, these function blocks are implemented using look-up tables (LUTs). The LAB has combinatorial and registered outputs. The LAB also contains storage blocks (691) for implementing sequential or registered logic functions. The LAB has a carry chain for implementing logic functions requiring carry bits. The LAB may also be configured to implement a random access memory.
ABSTRACT WORD COUNT: 172

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 961211 A2 Published application (A1with Search Report ;A2without Search Report)
Search Report: 971119 A3 Separate publication of the European or International search report
Examination: 980617 A2 Date of filing of request for examination: 980422
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	810
SPEC A	(English)	EPAB96	12528
Total word count - document A			13338
Total word count - document B			0

Total word count - documents A + B 13338

32/5/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00572668
Programmable logic **array integrated** circuit **with cascade connections between** logic modules
Integrierte Schaltung einer programmierbaren logischen Anordnung mit kaskadierten Anschlussen zwischen logischen Modulen
Circuit integre a reseau logique programmable avec connexion en cascade entre modules logiques
PATENT ASSIGNEE:
ALTERA CORPORATION, (398571), 2610 Orchard Parkway, San Jose, California 95134-2020, (US), (applicant designated states: BE;DE;DK;ES;FR;GB;GR;IE;IT;LU;NL;PT)
INVENTOR:
Cliff, Richard G. , 192 Smithwood Street, Milpitas, CA 95035, (US)
Ahanin, Bahram, 10550 South Foothill Boulevard, Cupertino, CA 95014, (US
LEGAL REPRESENTATIVE:
Adkins, Michael (42842), Withers & Rogers 4 Dyer's Buildings Holborn, London EC1N 2JT, (GB)
PATENT (CC, No, Kind, Date): EP 569134 A2 931110 (Basic)
EP 569134 A3 940216
EP 569134 B1 970806
APPLICATION (CC, No, Date): EP 93302742 930407;
PRIORITY (CC, No, Date): US 880888 920508
DESIGNATED STATES: BE; DE; DK; ES; FR; GB; GR; IE; IT; LU; NL; PT
INTERNATIONAL PATENT CLASS: H03K-019/177;
CITED PATENTS (EP A): EP 415542 A; EP 177261 A
CITED REFERENCES (EP A):
EDN ELECTRICAL DESIGN NEWS vol. 34, no. 20 , 28 September 1989 , NEWTON, MASSACHUSETTS US pages 91, 93, 94, 96, 98, 100 , XP000067462 D. CONNER 'PLD Architectures Require Scrutiny';

ABSTRACT EP 569134 A2
A **programmable logic** array integrated **circuit** has a number of relatively simple **logic modules** (12) which can be interconnected in any of a wide variety of ways via a general purpose interconnection network to enable the circuit to perform logic functions which can be quite complex. In addition, at least some of the **logic modules** are connectable to one another by cascade connections (72a,72b,48) and include additional logic elements for logically combining the outputs of the cascade connected modules so that modules can be concatenated to perform relatively complex logic functions without always having to make use of the general purpose interconnection network. (see image in original document)
ABSTRACT WORD COUNT: 110

LEGAL STATUS (Type, Pub Date, Kind, Text):
Lapse: 010103 B1 Date of lapse of European Patent in a contracting state (Country, date): BE 19970806, DE 19971107, DK 19970806, FR 19980102, GR 19970806, IE 19980407, IT 19970806, LU 19980430, PT 19971111,
Lapse: 20000202 B1 Date of lapse of European Patent in a contracting state (Country, date): BE 19970806, DE 19971107, DK 19970806, FR 19980102, GR 19970806, IT 19970806, LU 19980430, PT 19971111,
Application: 931110 A2 Published application (A1with Search Report ;A2without Search Report)
Lapse: 20000216 B1 Date of lapse of European Patent in a contracting state (Country, date): BE

			19970806, DE 19971107, DK 19970806, FR 19980102, GR 19970806, IT 19970806, LU 19980430, PT 19971111,
Search Report:	940216	A3	Separate publication of the European or International search report
Examination:	940928	A2	Date of filing of request for examination: 940802
Examination:	951102	A2	Date of despatch of first examination report: 950918
Grant:	970806	B1	Granted patent
Lapse:	980408	B1	Date of lapse of the European patent in a Contracting State: DE 971107
Lapse:	980520	B1	Date of lapse of the European patent in a Contracting State: BE 970806, DE 971107
Lapse:	980610	B1	Date of lapse of the European patent in a Contracting State: BE 970806, DE 971107, PT 971111
Lapse:	980722	B1	Date of lapse of the European patent in a Contracting State: BE 970806, DE 971107, DK 970806, PT 971111
Oppn None:	980729	B1	No opposition filed
Lapse:	980826	B1	Date of lapse of the European patent in a Contracting State: BE 970806, DE 971107, DK 970806, FR 980102, PT 971111
Lapse:	991020	B1	Date of lapse of European Patent in a contracting state (Country, date): BE 19970806, DE 19971107, DK 19970806, FR 19980102, IT 19970806, PT 19971111,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	644
CLAIMS B	(English)	9708W1	670
CLAIMS B	(German)	9708W1	596
CLAIMS B	(French)	9708W1	743
SPEC A	(English)	EPABF1	2355
SPEC B	(English)	9708W1	2486
Total word count - document A			2999
Total word count - document B			4495
Total word count - documents A + B			7494

32/5/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00372051
Semiconductor integrated circuit.
Integrierte Halbleiterschaltung.
Circuit integre semi-conducteur.
PATENT ASSIGNEE:
Pilkington Micro-Electronics Limited, (790700), Prescot Road St. Helens, Merseyside WA10 3TT, (GB), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Cliff, Richard Guy Maud Cottage , 68 Underwood Road Plimpton, Plymouth Devon PL7 3FZ, (GB)
Austin, Kenneth, 226B Chester Road Hartford, Northwich Cheshire, (GB
LEGAL REPRESENTATIVE:
Driver, Virginia Rozanne et al (58902), Page White & Farrer 54 Doughty Street, London WC1N 2LS, (GB)
PATENT (CC, No, Kind, Date): EP 372749 A2 900613 (Basic)
EP 372749 A3 900801
EP 372749 B1 940921
APPLICATION (CC, No, Date): EP 89312115 891122;
PRIORITY (CC, No, Date): GB 8828828 881209

DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: H03K-019/173;
CITED PATENTS (EP A): GB 2202356 A; GB 2202356 A; GB 2171546 A; GB 2171546 A; GB 2180382 A; GB 2138188 A

ABSTRACT EP 372749 A2

This invention is concerned with semiconductor integrated circuits of the type comprising configurable **logic circuit** arrays of the type disclosed in specification No. GB B-2180382. Such an array may be programmed to configure a plurality of NAND-gates (G1) in the array to perform various and different logic functions. This invention is particularly concerned with the provision of an additional **logic circuit** (c) at each discrete site or cell which additional **logic circuit** (c) is controllable by a control means (GCS) to cause the additional **logic circuit** (c) and the **logic circuit** to operate as either a simple NAND logic function or a simple LATCH logic function.

ABSTRACT WORD COUNT: 110

```
File 238:Abs. in New Tech & Eng. 1981-2001/Jun
         (c) 2001 Reed-Elsevier (UK) Ltd.
File 108:AEROSPACE DATABASE 1962-2001/JUN
         (c) 2001 AIAA
File   8:Ei Compendex(R) 1970-2001/Jun W4
         (c) 2001 Engineering Info. Inc.
File  77:Conference Papers Index 1973-2001/Jul
         (c) 2001 Cambridge Sci Abs
File  35:Dissertation Abs Online 1861-2001/Jul
         (c) 2001 ProQuest Info&Learning
File 202:Information Science Abs. 1966-2001/ISSUE 04
         (c) Information Today, Inc
File  65:Inside Conferences 1993-2001/Jul W1
         (c) 2001 BLDSC all rts. reserv.
File   2:INSPEC 1969-2001/Jul W1
         (c) 2001 Institution of Electrical Engineers
File  14:Mechanical Engineering Abs 1973-2001/May
         (c) 2001 Cambridge Sci Abs
File 233:Internet & Personal Comp. Abs. 1981-2001/Jun
         (c) 2001 Info. Today Inc.
File  94:JICST-EPlus 1985-2001/Jun W2
         (c)2001 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2001/Jun 29
         (c) 2001 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2001/Jul 02
         (c) 2001 ProQuest Info&Learning
File   6:NTIS 1964-2001/Jul W3
         Comp&distr  2000 NTIS, Intl Cpyrght All Right
File 144:Pascal 1973-2001/Jul W1
         (c) 2001 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2001/Jul W1
         (c) 2001 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2001/May
         (c) 2001 The HW Wilson Co.
File 583:Gale Group Globalbase(TM) 1986-2001/Jul 02
         (c) 2001 The Gale Group
File 266:FEDRIP 2001/Jun
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  62:SPIN(R) 1975-2001/Apr W3
         (c) 2001 American Institute of Physics
File 239:Mathsci 1940-2001/Aug
         (c) 2001 American Mathematical Society

Set     Items   Description
S1      17475   PROGRAMMABLE(2W)LOGIC?
S2      16183   SPLD? ? OR CPLD? ? OR FPGA? ? OR FPIC? ? OR FIELD()PROGRAM-
             MABLE()(GATE? ? OR INTERCONNECT? ? OR INTER()CONNECT? ?)
S3      88763   LOGIC?(2W)(UNIT? ? OR DEVICE? ? OR CIRCUIT?? OR MICROCIRCU-
             IT? ? OR CHIP? ? OR MODULE? ? OR BOARD? ? OR BLOCK? ? OR MICR-
             OCHIP? ? OR IC OR APPARATUS)
S4     782206   RAM? ? OR MEMOR???
S5        819   READ?(5N)PORT? ?
S6        470   WRIT???(5N)PORT? ?
S7      14514   SINGLEPORT? ? OR (SINGLE OR ONE OR 1)(5N)PORT? ?
S8      33428   DUALPORT? ? OR (DUAL OR TWO OR 2 OR MULTIPLE OR MULTI OR D-
             UAL OR SEPARATE OR DIFFERENT OR TWIN OR SECOND? OR DOUBLE)(5N-
             )PORT? ? OR MULTIPORT? ?
S9         22   S1:S2 AND ((S5 AND S6) OR (S7 AND S8))
S10        13   RD (unique items)
S11        88   S3 AND ((S5 AND S6) OR (S7 AND S8))
S12        44   S11 AND S4
S13        37   RD (unique items)
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S14	33	S13 NOT S10

10/5/1 (Item 1 from file: 108)
DIALOG(R)File 108:AEROSPACE DATABASE

01558364 N84-33055
Programmable **arithmetic** logic **unit**
Patent
MILLER, G. I., inventor (to Air Force)
Department of the Air Force, Washington, DC.
CORPORATE CODE: DM389242
Jun. 1984 4P.
ANNOUNCEMENTS: Supersedes AD-D009495
REPORT NO.: AD-D011128
PATENT INFO.: US-PATENT-4,454,589; US-PATENT-APPL-SN-357440; US-PATENT-CLASS-364-716
LANGUAGE: English
COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States
DOCUMENT TYPE: PATENT
DOCUMENTS AVAILABLE FROM AIAA Technical Library
OTHER AVAILABILITY: US Patent and Trademark Office
JOURNAL ANNOUNCEMENT: STAR8422
A **programmable** arithmetic **logic** unit for performing high speed bit sliced, pipelined computations at very low power is fabricated as a LSI component using CMOS/SOS technology. It is microprogrammable and operates in conjunction with a fast microprogram store program memory and controller. **Dual** input **ports** which supply data from eight sources are latched and operated on while new data is simultaneously fetched. Instruction bits shift data in either port left or right, select complements and select an operand between device input and output data in **one port** . The data processed in each port is compared and is added to provide a latched tri-state output to an external device (Author (GRA))
SOURCE OF ABSTRACT/SUBFILE: DTIC
DESCRIPTORS: *ARITHMETIC AND LOGIC UNITS; *CMOS; *LARGE SCALE INTEGRATION ; *MICROPROGRAMMING; *PIPELINING (COMPUTERS); COMPUTER STORAGE DEVICES; CONTROLLERS; HIGH SPEED; INPUT/OUTPUT ROUTINES; LOGIC CIRCUITS; PATENTS; POWER EFFICIENCY; SIGNAL PROCESSING
SUBJECT CLASSIFICATION: 7560 Computer Operations & Hardware (1975-)
COSATI CODE: 9B Fluidics and Fluerics

10/5/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05616551 E.I. No: EIP00085271698
Title: Effects of Spar coupled analysis
Author: Gupta, Himanshu; Finn, Lyle; Weaver, Tim
Corporate Source: Spars Int Inc
Conference Title: 32nd Annual Offshore Technology Conference - OTC 2000
Conference Location: Houston, TX, USA Conference Date: 19000501-19000504
E.I. Conference No.: 57001
Source: Proceedings of the Annual Offshore Technology Conference v 2 2000. Offshore Technol Conf, USA. p 629-638
Publication Year: 2000
CODEN: OSTCBA ISSN: 0160-3663
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)
Journal Announcement: 0009W2
Abstract: This paper presents a discussion of the effect of including mooring line dynamics and riser **friction** on Spar response. Data from the Neptune Spar revealed that the heave motion of the vessel was considerably less than predicted by an uncoupled analysis. It was believed that the **primary cause** of the reduced **heave** was damping **forces such** as friction between the risers and the supporting guides and mooring line

dynamic **drag that** were unaccounted for. A new analysis capability was subsequently developed to simultaneously predict the dynamic response of the vessel, mooring lines, and risers. Results of the coupled analysis reveal that mooring line dynamics and riser friction have significant effect on the Spar heave response. In this paper, comparison of **coupled analysis** results to Neptune Spar motions during Hurricane Georges will be **presented . As** a result of reduction in heave response, the **draft of** the Spar can be reduced. A coupled analysis of a shorter draft Spar is presented. Results for matthieu's instability problem, effect of coupling in different water depths and comparison of coupled response of classic versus truss Spar configurations are also presented. Coupled response of Spar and a second vessel moored together with chains is presented to demonstrate the multiple vessel simulation capability of the coupled analysis program. (Author abstract) 3 Refs.

Descriptors: **Offshore structures ; Semisubmersibles** ; Computer simulation; Finite element method; Mooring cables; Friction; Marine risers; Drag; Dynamic response; Hurricanes

Identifiers: Coupled analysis; Semisubmersible **platforms ; Coulomb** friction; Software Package ABASIM

Classification Codes:

674.2 (Marine Drilling Rigs & Platforms); 674.1 (Small Marine Craft); 723.5 (Computer Applications); 921.6 (Numerical Methods); 671.2 (Ship Equipment)

674 (Other Marine Craft); 723 (Computer Software); 921 (Applied Mathematics); 472 (Ocean Engineering); 671 (Naval Architecture)

67 (MARINE ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS); 47 (OCEAN TECHNOLOGY)

10/5/3 (Item 2 from file: 8)

04566133 E.I. No: EIP96113428161

Title: Use of multi - port **memories in programmable structures for architectural synthesis**

Author: Mandal, C.; Zimmer, R.M.

Corporate Source: Brunel Univ, Uxbridge, UK

Conference Title: Proceedings of the 1996 8th Annual IEEE International Conference on Innovative Systems in Silicon

Conference Location: Austin, TX, USA Conference Date: 19961009-19961011

Sponsor: IEEE

E.I. Conference No.: 45644

Source: Proceedings of the Annual IEEE International Conference on Innovative Systems in Silicon 1996. IEEE, Piscataway, NJ, USA,96CH35996. p 341-351

Publication Year: 1996

CODEN: 002487 ISSN: 1063-2204

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9701W3

Abstract: In this paper we make a study of the capabilities required of memories to support the synthesis of designs using structured architectures. We explore the advantages of using **multi -port** memories with **two** write **ports** as an architectural component over conventional memories with a **single** write **port** in such a synthesis environment. A study the of the memory resources available in some of the current **Field Programmable Gate** Arrays (**FPGA**) is made. We then propose a **multi - port** memory structure that could be suitable for use in programmable structures such as **FPGAs** , to facilitate implementations of designs through HLS. The principal advantages of the proposed memory structure are its flexibility, simplicity and its ability to support more efficient execution of operations than existing memory structures. (Author abstract) 14 Refs.

Descriptors: *Semiconductor storage; Logic gates; Computer architecture; Logic design; VLSI circuits; Algorithms; Integrated circuit layout;

Electric network synthesis
Identifiers: High level synthesis; **Field programmable gate** array (**FPGA**)
Classification Codes:
722.1 (Data Storage, Equipment & Techniques); 712.1 (Semiconducting Materials); 714.2 (Semiconductor Devices & Integrated Circuits); 721.2 (Logic Elements); 721.3 (Computer Circuits)
722 (Computer Hardware); 712 (Electronic & Thermionic Materials); 714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

10/5/4 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04464975 E.I. No: EIP96083273378
Title: New generation of ORCA FPGA with enhanced features and performance
Author: Ngai, T.; Singh, S.; Britton, B.K.; Leung, W.-B.; Nguyen, H.; Powell, G.P.; Albu, R.; Andrews, W.B.; He, J.; Spivak, C.W.
Corporate Source: AT&T Microelectronics, Allentown, PA, USA
Conference Title: Proceedings of the 1996 IEEE Custom Integrated Circuits Conference
Conference Location: San Diego, CA, USA Conference Date: 19960505-19960508
Sponsor: IEEE
E.I. Conference No.: 45104
Source: Proceedings of the Custom Integrated Circuits Conference 1996. IEEE, Piscataway, NJ, USA,96CH35886. p 247-250
Publication Year: 1996
CODEN: PCICER ISSN: 0886-5930
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9610W1
Abstract: This paper describes the new AT&T Optimized Reconfigurable Cell Array (ORCA) 2CA and 2TA series of **Field -Programmable Gate** Arrays (**FPGAs**). Both series are based on the ORCA 2C/T architecture, but migrated to the advanced AT&T 0.35 mu CMOS processes. These two processes are individually optimized for 5V and 3.3V operations. In addition, architectural innovations are incorporated into the new series to enhance both performance and functionality. These include: Efficient support of parallel multiplier Efficient support of synchronous **single -port** and **dual -port** memories Streamlined creation of large memory using port-enable control and internal tristate buffers Easy system integration with the 5V-tolerant input/output buffers, found on the 3.3V 2TA series. As the result, the ORCA 2CA/2TA arrays are significantly smaller and 15%/30% faster (PFU speed) than the corresponding 0.5 mu 2C/T arrays. (Author abstract) 4 Refs.
Descriptors: *Logic circuits; Application specific integrated circuits; CMOS integrated circuits; Optimization; Multiplying circuits; Semiconductor storage; Buffer storage
Identifiers: Optimized reconfigurable cell array; Field programmable cell arrays; Parallel multiplier; Synchronous memories
Classification Codes:
721.2 (Logic Elements); 714.2 (Semiconductor Devices & Integrated Circuits); 921.5 (Optimization Techniques); 721.3 (Computer Circuits); 722.1 (Data Storage, Equipment & Techniques)
721 (Computer Circuits & Logic Elements); 714 (Electronic Components); 921 (Applied Mathematics); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

10/5/5 (Item 4 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

03390225 E.I. Monthly No: EI9203030622
Title: PSD301 programmable peripheral with memory for microcontroller and embedded microprocessor applications.
Author: Jay, Chris
Corporate Source: WSI, Fremont, CA, USA
Source: Microprocessors and Microsystems v 15 n 6 Jul-Aug 1991 p 333-341
Publication Year: 1991
CODEN: MIMID5 ISSN: 0141-9331
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9203
Abstract: A little more than a decade ago the systems designer had to construct all I/O devices out of basic TTL logic elements. Since the mid 1970s semiconductor manufacturers have provided special-purpose interface devices ranging from parallel and serial ports to floppy disc controllers. These LSI peripherals are programmable in the sense that their operational parameters are user selectable (e.g., a serial port might have a programmable baud rate, number of bits/character, interrupt characteristics etc.). Following developments in **programmable logic** , a new generation of programmable peripherals is beginning to appear. These peripherals can be programmed to handle almost any type of I/O transaction. This application note from WSI describes the versatile PSD301 programmable peripheral. The PSD301 has two 8-bit ports plus a 3-bit **port** , together with on-chip **read /write** and read-only memory. (Author abstract) 5 Refs.
Descriptors: *COMPUTER PERIPHERAL EQUIPMENT--*Performance; LOGIC CIRCUITS, TRANSISTOR TRANSISTOR; LOGIC DEVICES; INTEGRATED CIRCUITS, LSI; DATA STORAGE, DIGITAL; COMPUTERS, MICROCOMPUTER
Identifiers: MICROCONTROLLERS; TTL LOGIC ELEMENTS; LSI PERIPHERALS
Classification Codes:
722 (Computer Hardware); 713 (Electronic Circuits); 714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

10/5/6 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01441245 ORDER NO: AADAA-IMM96242
AN SRAM-PROGRAMMABLE FIELD-RECONFIGURABLE MEMORY
Author: NGAI, KAI-KIT TONY
Degree: M.A.SC.
Year: 1994
Corporate Source/Institution: UNIVERSITY OF TORONTO (CANADA) (0779)
Adviser: J. ROSE
Source: VOLUME 33/06 of MASTERS ABSTRACTS.
PAGE 1940. 83 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544
ISBN: 0-315-96242-9

Field -programmable gate arrays (**FPGAs**) are now widely used for implementing digital logic, but most **FPGAs** have little or no on-chip memory. Those **FPGAs** that do have memory capability suffer from either poor memory density and speed or insufficient flexibility to form different kinds of memories. The flexibility of the memory in **FPGAs** is key because each application circuit typically needs a different number of distinct memories, each with different aspect ratios. This thesis describes the design and implementation of an SRAM-programmable field-reconfigurable memory (FRM), which has the flexibility to form over two hundred different memory configurations, each with up to four individual memories. A novel

feature of the memory is that is can be used to form a pseudo **dual -port** memory, which supports **dual -port reading** and **single -port** exclusive **writing** . This field-reconfigurable memory has four 1kb memory blocks and each of them can be configured into four different aspect ratios. It requires just 40 configuration bits and is only 38% larger and 89% slower than the ASIC memory it is based upon. Compared to memory implemented usign the Xilinx 4000 series internal memory, the FRM has 16 to 23 times greater memory density and is two to three times faster. This is achieved by employing a novel mapping circuit to improve low-level flexibility and utilizing a memory-tuned hierarchical routing architecture with intelligent wire grouping to optimize overall speed and density. Although this is a stand-alone FRM implementation, the design can be embedded inside an **FPGA** .

10/5/7 (Item 1 from file: 202)
DIALOG(R)File 202:Information Science Abs.

00123989 8803989
ISA Document Number in Printed Publication: 8804312
Microcode testing of PLA's in a data processor.
Document Type: Patent
Author (Affiliation): Aaron, R.W.; Kuban, J.; MacGregor, D.B.; Thompson, R.R.
Patent Assignee(s): Motorola, Inc.
Patent Number(s): US 4745574
Publication Language(s): English
Source: May 17, 1988

In a microcoded data processor having: an address port for providing addresses; an operand port for receiving instructions and data; an instruction register for temporarily storing each of said instructions; and at least one PLA for decoding the instruction in the instruction register and providing a plurality of outputs in response thereto; a method for recursively testing the PLA comprising the steps of: accepting as an instruction operand a selected test value via the operand port; loading said selected test value into said instruction register; allowing said PLA to decode said selected test value as if it were one of said instructions and to provide said plurality of outputs in response thereto; extracting a selected portion of said plurality of outputs provided by said PLA in response to the decoding of said selected test value; and providing as if it were an instruction address said extracted portion of said plurality of outputs of said PLA via said address port; whereby the PLA may be tested by: (1) providing a predetermined sequence of said selected test values to said data processor via said operand **port** ; and (2) comparing each of said instruction addresses provided by said data processor via said address **port** to a selected **one** of a plurality of expected values; so that the PLA can be tested by using only said address and said operand ports.

Descriptors: PLA'S (**PROGRAMMABLE LOGIC** ARRAYS); **PROGRAMMABLE LOGIC** ARRAYS (PLA'S); CODES; DATA PROCESSORS; DATA TRANSMISSION; MICROPROGRAMS; PATENTS; TESTING
Subject Class Header (Number):Information Generation and Promulgation, Communications and Telecommunications Systems (03.11)

10/5/8 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6865684 INSPEC Abstract Number: B2001-04-1265A-077, C2001-04-5210B-028
Title: Heterogeneous technology mapping for FPGAs **with** dual- port **embedded memory arrays**
Author(s): Wilton, S.J.E.
Author Affiliation: Dept. of Electr. & Comput. Eng., British Columbia

Univ., Vancouver, BC, Canada
Conference Title: FPGA'00. ACM/SIGDA International Symposium on Field Programmable Gate Arrays p.67-74
Publisher: ACM, New York, NY, USA
Publication Date: 2000 Country of Publication: USA vii+223 pp.
ISBN: 1 58113 193 3 Material Identity Number: XX-2000-00398
U.S. Copyright Clearance Center Code: 1 58113 193 3/2000/02...$5.00
Conference Title: Proceedings of FPGA2000: ACM/SIGDA International Symposium on Field Programmable Gate Arrays
Conference Sponsor: ACM
Conference Date: 9-11 Feb. 2000 Conference Location: Monterey, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: It has become clear that on-chip storage is an essential component of high-density **FPGAs** . These arrays were originally intended to implement storage, but recent work has shown that they can also be used to implement logic very efficiently. This previous work has only considered **single -port** arrays. Many current **FPGAs** , however contain **dual -port** arrays. In this paper we present an algorithm that maps logic to these **dual -port** arrays. Our algorithm can either optimize area with no regard for circuit speed, or optimize area under the constraint that the combinational depth of the circuit does not increase. Experimental results show that, on average, our algorithm packs between 29% and 35% more logic than an algorithm that targets **single - port** arrays. We also show, however that even with this algorithm, **dual -port** arrays are still not as area-efficient as **single -port** arrays when implementing logic. (15 Refs)
Subfile: B C
Descriptors: **field programmable gate** arrays; logic CAD
Identifiers: heterogeneous technology mapping; **FPGAs** ; **dual -port** embedded memory arrays; on-chip storage; **dual -port** arrays
Class Codes: B1265A (Digital circuit design, modelling and testing); B1265B (Logic circuits); C5210B (Computer-aided logic design); C7410D (Electronic engineering computing); C5120 (Logic and switching circuits)

10/5/9 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6727973 INSPEC Abstract Number: B2000-11-6210L-183, C2000-11-5620L-035
Title: A local area system network RHiNET-1: a network for high performance parallel computing
Author(s): Nishi, H.; Tasho, K.; Yamamoto, J.; Kudoh, T.; Amano, H.
Conference Title: Proceedings the Ninth International Symposium on High-Performance Distributed Computing p.296-7
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 2000 Country of Publication: USA xi+316 pp.
ISBN: 0 7695 0783 2 Material Identity Number: XX-2000-01982
U.S. Copyright Clearance Center Code: 1082-8907/2000/$10.00
Conference Title: Proceedings the Ninth International Symposium on High-Performance Distributed Computing
Conference Sponsor: IEEE Comput. Soc Tech. Committee on Distributed Process.; Univ. Arizona ECE Dept
Conference Date: 1-4 Aug. 2000 Conference Location: Pittsburgh, PA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The Real World Computing Partnership (RWCP) has developed a local area system network (LASN) called RHiNET-1 (RWCP High-performance NETwork, version 1) using 1.33-Gbps optical interconnections for high-performance computing using personal computers distributed in an office or laboratory environment. The network interface, RHiNET-1/NI, uses a complex **programmable logic** device (**CPLD**) based protocol controller to provide an easy evaluation platform for various protocols. It fits in a

32-bit/33-MHz PCI bus. The switch, RHiNET-1/SW, consists of a single-chip CMOS switch and external SRAM. It provides low-latency, reliable communication with a flexible topology design. We are currently evaluating protocols on RHiNET-1. RHiNET-1 will enable a new form of high-performance computing environment. We are also developing the second implementation, RHiNET-2. RHiNET-2/NI will support a 64-bit/66-MHz PCI bus. RHiNET-2 /SW is an 8-Gbps/**port** 8*8 **single** -chip ASIC switch. The aggregate bandwidth of RHiNET-2/SW is 64 Gbps. (3 Refs)

Subfile: B C

Descriptors: CMOS integrated circuits; local area networks; network interfaces; optical interconnections; parallel processing; **programmable logic** devices; protocols; SRAM chips; switches; system buses

Identifiers: RHiNET-1; local area system network; high-performance parallel computing; Real World Computing Partnership; RWCP high-performance network; optical interconnections; distributed personal computers; network interface; complex **programmable logic** device; **CPLD** -based protocol controller; protocol evaluation platform; single-chip CMOS switch; external SRAM; low-latency reliable communication; flexible topology design; PCI bus ; single-chip ASIC switch; bandwidth; 1.33 Gbit/s; 32 bit/s; 33 MHz

Class Codes: B6210L (Computer communications); B4270 (Integrated optoelectronics); C5620L (Local area networks); C5440 (Multiprocessing systems); C5610N (Network interfaces); C5610S (System buses)

Numerical Indexing: bit rate 1.33E+09 bit/s; bit rate 3.2E+01 bit/s; frequency 3.3E+07 Hz

10/5/10 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

6566132 INSPEC Abstract Number: B2000-05-1265B-089, C2000-05-7410D-133

Title: Logical-to-physical memory mapping for FPGAs **with** dual- port **embedded arrays**

Author(s): Ho, W.K.C.; Wilton, S.J.E.

Author Affiliation: Dept. of Electr. & Comput. Eng., British Columbia Univ., Vancouver, BC, Canada

Conference Title: Field Programmable Logic and Applications. 9th International Workshop, FPL'99. Proceedings (Lecture Notes in Computer Science Vol.1673) p.111-23

Editor(s): Lysaght, P.; Irvine, J.; Hartenstein, R.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 1999 Country of Publication: Germany xi+541 pp.

ISBN: 3 540 66457 2 Material Identity Number: XX-1999-02846

Conference Title: Field Programmable Logic and Applications. 9th International Workshop, FPL'99. Proceedings

Conference Date: 30 Aug.-1 Sept. 1999 Conference Location: Glasgow, UK

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: On-chip storage has become critical in large **FPGAs** . This has led most **FPGA** vendors to include configurable embedded arrays in their devices. Because of the large number of ways in which the arrays can be combined, and because of the configurability of each array, there are often many ways to implement the memories required by a circuit. Implementing user memories using physical arrays is called logical-to-physical mapping, and has previously been studied for **single -port FPGA** memory arrays. Most current **FPGAs** , however, contain **dual -port** arrays. In this paper, we present a logical-to-physical algorithm that specifically targets **dual - port FPGA** arrays. We show that this algorithm results in 28% denser memory implementations than the only previously published algorithm. (14 Refs)

Subfile: B C

Descriptors: circuit layout CAD; **field programmable gate** arrays; real-time systems

Identifiers: logical-to-physical memory mapping; **FPGAs ; dual -port** embedded arrays; on-chip storage; configurable embedded arrays;

configurability; user memories; physical arrays; **single -port FPGA** memory arrays; **dual -port** arrays
Class Codes: B1265B (Logic circuits); B1265A (Digital circuit design, modelling and testing); C7410D (Electronic engineering computing); C5120 (Logic and switching circuits)

10/5/11 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6029274 INSPEC Abstract Number: B9811-1265B-006, C9811-5120-001
Title: FPGA **devices of up to 40000 gates**
Author(s): Zannoli, S.
Journal: Elettronica Oggi no.255 p.83-5
Publisher: Gruppo Editoriale Jackson,
Publication Date: 15 May 1998 Country of Publication: Italy
CODEN: ELOGDA ISSN: 0391-6391
SICI: 0391-6391(19980515)255L.83:FD4G;1-Z
Material Identity Number: E252-98009
Language: Italian Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The A3200Dx device offers in a **single** chip a 100 MHz **double port** SRAM, a wide decoder of controllable speed, high speed datapath circuitry, up to 40000 gates and Jtag boundary testing with the ability to debug in real time. The system architecture is described and the possibilities of integration with other circuits are outlined. (0 Refs)
Subfile: B C
Descriptors: boundary scan testing; **field programmable gate** arrays; logic testing
Identifiers: **FPGA** devices; A3200Dx device; **double port** SRAM; controllable speed decoder; high speed datapath circuitry; Jtag boundary testing; real time debug; system architecture; 100 MHz
Class Codes: B1265B (Logic circuits); B7210B (Automatic test and measurement systems); C5120 (Logic and switching circuits); C5210B (Computer-aided logic design)
Numerical Indexing: frequency 1.0E+08 Hz

10/5/12 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

03875170 INSPEC Abstract Number: B91031998, C91028410
Title: Programmable logic **gate array and its applications to reconfigurable network based on modified sign digit**
Author(s): Suzaki, Y.; Yatagai, T.
Author Affiliation: Inst. of Appl. Phys., Tsukuba Univ., Ibaraki, Japan
Conference Title: Optical Computing 1989 Technical Digest Series, Vol.9. Postconference Edition. Summaries of Papers Presented at the Optical Computing Topical Meeting p.370-3
Publisher: Opt. Soc. America, Washington, DC, USA
Publication Date: 1989 Country of Publication: USA xi+446 pp.
Conference Sponsor: OSA; NSF; et al
Conference Date: 27 Feb.-1 March 1989. Conference Location: Salt Lake City, UT, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The authors have developed a **programmable** parallel **logic** unit with a dynamic interconnection ability based on the truth table architecture. This enables them to design very flexible digital optical computing systems. The element cell is able to select which output ports are active or not. Because of this, the interconnection network is dynamically configured. It is convenient to use ternary logic to assign

one or **two** of three **ports** to the output port. Ternary logic is also employed to make a prototype electrooptic gate and perform a modified sign digit (MSD) operation, which enables the authors to make a full parallel algorithm of numerical calculations. (0 Refs)
Subfile: B C
Descriptors: optical information processing; optical logic; parallel algorithms; parallel architectures; ternary logic
Identifiers: logic gate array; reconfigurable network; modified sign digit; **programmable** parallel **logic** unit; dynamic interconnection ability; truth table architecture; flexible digital optical computing systems; element cell; output ports; ternary logic; electrooptic gate; parallel algorithm; numerical calculations
Class Codes: B4180 (Optical logic devices and optical computing techniques); C5110D (Optical logic elements); C5270 (Optical computing techniques); C5220 (Computer architecture)

10/5/13 (Item 1 from file: 99)

2215192 H.W. WILSON RECORD NUMBER: BAST00074718
FPGA **makes simple FIFO**
Brugolaras, Luis Miguel;
EDN v. 45 no22 (Oct. 26 2000) p. 162-4
DOCUMENT TYPE: Feature Article ISSN: 0012-7515 LANGUAGE: English
RECORD STATUS: Corrected or revised record

ABSTRACT: An **FPGA** -based, synchronous first-in, first-out (FIFO) scheme that makes it easy to determine FIFO occupancy is presented. The circuit is implemented in a demultiplexer that writes data in the FIFO when the data arrives and reads data, depending on FIFO occupancy. The circuit employs a 16 bit dual-**port** RAM macro, **read** -and **write** -address counters, and a flag processor. In another proposal, FIFO occupancy can also be read using an up/down counter controlled by read- and write-enabled clocks.

DESCRIPTORS: **Field programmable gate** arrays--Design; First-in first-out queues;

14/TI/1 (Item 1 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: A new memory-based FFT processor for VDSL transceivers

14/TI/2 (Item 2 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: Fully-parallel 25 MHz 2.5 Mb CAM

14/TI/3 (Item 3 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: Special and embedded memory macrocells for low-cost and low-power in MPEG environment

14/TI/4 (Item 4 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: Design of the basic cell and metallized RAM for 0.5 mu m CMOS gate array

14/TI/5 (Item 5 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: Special memory and embedded memory macros in MPEG environment

14/TI/6 (Item 6 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: 14-port 3.8 ns 116-word 64 b read-renaming register file

14/TI/7 (Item 7 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: A sub-micron CMOS embedded SRAM compiler.

14/TI/8 (Item 8 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: A submicrometer CMOS embedded SRAM compiler.

14/TI/9 (Item 9 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: A 5 ns 369 kb port-configurable embedded SRAM with 0.5 mu m CMOS gate array.

14/TI/10 (Item 10 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: Dual- port RAMs simplify processor communications.

14/TI/11 (Item 11 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: SUB-FIVE NANOSECOND ECL 128 X 18 THREE PORT REGISTER FILE.

14/TI/12 (Item 12 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: ECL MEMORY **CELL WITH SEPARATE** READ **AND** WRITE PORTS.

14/TI/13 (Item 13 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: HM53462:64 kbit X 4 DUAL- PORT **VIDEO** RAM **WITH LOGIC FUNCTIONS.**

14/TI/14 (Item 14 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: THREE-PORT LATCH.

14/TI/15 (Item 15 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

Title: MULTIPORT REGISTER FILE STREAMLINES SIGNAL PROCESSING.

14/TI/16 (Item 16 from file: 8)
DIALOG(R)File 8:(c) 2001 Engineering Info. Inc. All rts. reserv.

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Random pattern testability of memory **address logic**

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